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Final Technical Report
August 1977

HIGH POWER CONTROLLER AND ICS

General Atronics Corporation, a subsidiary of
The Magnovox Government & Industrial Electronics Co.

Approved for public release; distribution unlimited.

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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Higher power, all-electronic HF, LF and VLF amplitude and phase controllers are surveyed for use in adaptive Interference Cancellation Systems (ICS).

A two-channel HF ICS breadboard is designed and built for use at high power. While the testing is general, one area of particular interest is simultaneous transmission and reception at frequency spacings too close to be realizable with filters.

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The system aspects of the HFICS are covered in some detail. In view of the limitations of both the HFICS and the transceivers with which it may be used, it is concluded that a single channel lower power version of the HFICS should prove of use in airborne applications.

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EVALUATION

The objective of this effort was to investigate the feasibility of high power (HF, LF, VLF) all electronic amplitude and phase controllers for use in Ground and Airborne Interference Cancellation Systems (ICS). The overall usefulness of the effort is to permit full duplex operation with less than 10% frequency separation between the transmit and receive frequencies for both ground and airborne applications. Preliminary testing has also revealed the usefulness of the ICS to permit simultaneous transmission and reception from [illegible] same antenna. The effort is in direct support of FY75 TPO No. 14 [illegible]omagnetic Compatibility. The experimental HF model was tested in an airborne environment the 24 May 1977 and additional ground and airborne testing is envisioned in the future.

Wayne E. Woodward

WAYNE E. WOODWARD
Project Engineer

SECTION 1 - INTRODUCTION

1.1 BACKGROUND

A requirement of many radio communications systems is the ability to simultaneously transmit and receive information. In many cases, this requirement has been impossible to meet because of the desensitization or even damage of the receiver front end caused by the high level signal coupled into the receiver antenna from a colocated transmitter. This is especially true on platforms such as aircraft and ships where R/T isolation by means of geographic spacing is not available.

The necessary proximity of LF, VLF, or HF antennas on an aircraft presents a severe interference problem in which transmission from the aircraft is picked up at a very high level on the aircraft's receiving antennas. The interference on the receiving antenna may be as strong as 100W, and cannot be rejected sufficiently by frequency filtering techniques. At HF, for example, the transmit and receive frequencies may be as close as 100 kHz, due to the problem of assigning a number of full-duplex circuits within the 2 MHz (approximate) window between the lowest usable frequency and the maximum usable frequency.

If it is not rejected by some means, the strong interference causes *desensitization* of the aircraft receiver. The desensitization problem would be mitigated if the interference could be rejected sufficiently. The effect of broadband transmitter noise falling in the receive channel would then become the limiting factor on receiver sensitivity.

Interference cancellation is a technique for suppressing, at a receiver input, energy which is coupled from a colocated transmitter. It has the advantage over frequency selective diplexing of being able to operate with minimal frequency spacing between transmit and receive frequencies, making it particularly useful where spectrum conservation is a requirement, or as in the case of the high frequency band, where the total available range of frequencies may not be sufficiently great to allow the 10% frequency spacing which is usually required for adequate isolation when provided by filtering.

Because the interference and noise are locally generated, they can be cancelled at the output of the receiving antenna by taking a portion of the transmitter output and adjusting its amplitude and phase so that when coherently combined with the receiving antenna output, the interference and noise are nulled. The amplitude and phase adjustment must match the coupling between the transmitting and receiving antennas. This coupling has slight variations due to motion of the antennas and flexing of the airframe and proximity of the runway during take-off and

landing. In order to provide a deep cancellation null, the amplitude and phase adjustments must be adaptively controlled to continually track the antenna coupling with high accuracy.

In addition, on take-off and landing, ground multipath causes the antenna coupling to vary even more severely and at a higher rate. Thus, the adaptive tracking circuits in the interference canceller must be capable of following these variations. Furthermore, a brief nulling time is desired when the interfering transmitter is first turned on. An HF ICS with a nulling time of 20 milliseconds is considered capable of providing the response time to meet both requirements. This nulling time is a factor of 20 faster than an earlier electromechanical HF ICS designed and fabricated by RADC/RBCT personnel, using two servo-driven quadrature goniometers to provide the amplitude and phase adjustment.

The unit providing the amplitude and phase adjustment is termed a signal controller. Designing an all-electronic signal controller which is capable of providing a sufficiently high level output to cancel a 50W interference is the crucial first step in designing the ICS. The most severe aspect of the high power requirements on the HF controller is linearity. Since the HF waveform is usually SSB, even a small nonlinearity in the controller will produce distortion components which are not cancelled by the interference on the receiving antenna.

All components used in the HF ICS must cover the four-octave HF band and operate without special tuning. Furthermore, in combination with the high power level and high linearity requirement, this broadband requirement has a strong influence on the selection of couplers, combiners, and splitters for use in the ICS.

Much of the prior work in interference cancellation has been confined to interferences received at relatively low power levels. At HF, LF and VLF high power transmitters are commonly used. This program is directed toward solving the interference cancellation problem under these more difficult conditions.

RADC has demonstrated the feasibility of building an HF canceller using servo-controlled variocouplers as the amplitude/phase controller. This system was excellent from the standpoint of freedom from distortion products. It shared the reliability problems common to electromechanical devices. As implemented, the frequency range was limited and the acquisition time was excessive. Neither of the latter problems are likely to prove insurmountable.

This effort was directed towards investigating all-electronic solutions to high level interference cancellation at VLF and LF and to implementing a dual channel Interference Cancellation System (ICS) at HF.

This report covers the design, development, and testing of an ICS for HF applications. The design included an extensive consideration of the application of the ICS to an HF radio system. It is shown that the sensitivity threshold of an HF receiver operating in the proximity of a high-level transmitter can be extended significantly by the use of an ICS, and that proper system design can relax the power handling requirements on the ICS controllers.

1.2 PRINCIPLES OF INTERFERENCE CANCELLATION SYSTEMS

The design principles of interference cancellation systems have been well established in previous developments [1,2]. The basic structure of an N-channel interference cancellation system (CIS) is shown in Figure 1. It operates on the principle that a replica of each interference to be cancelled from the receiving antenna output is locally available as an interference reference which may be adjusted in amplitude and phase to effect cancellation. This is indeed the case when the interferences are generated from local transmitters, each of whose outputs may be tapped to provide the references.

The amplitude and phase of each reference are adjusted by a controller, so that when all controller outputs are properly adjusted and coherently combined with the receiving antenna output, the interferences are cancelled at the ICS output. The controllers are adjusted by a stable, high gain feedback technique which uses a portion of the ICS output as a feedback control error signal. The input to each controller is correlated (multiplication followed by narrowband filtering) with the error signal, the result of which is amplified to provide the control signal to the controller.

Controllers may be implemented with an IF control signal [1] or with a DC control signal [2]. If control uses a mixer as the controller, operating the mixer so that its output varies linearly with either of the two inputs. Because of power limitations in the mixer, with linear operation, the IF approach is not suited to the control of high power signals. Further discussion, then, will be concentrated on DC control operation.

Amplitude and phase adjustments by DC control signals are most easily implemented by splitting the controller input into

[1] Abrams, B.S., *et al*, "Interference Cancellation: Volume I, Analysis and Breadboard Design," General Atronics Final Technical Report 2324-2626-15, prepared for Rome Air Development Center, under Contract F30602-73-C-0301, August 1973.

[2] Sauter, W.A. and R.N. Ghose, "Active Interference Cancellation System," American Nucleonics Corp. Final Technical Report, RADC-TR-69-41, April 1969. AD852786.

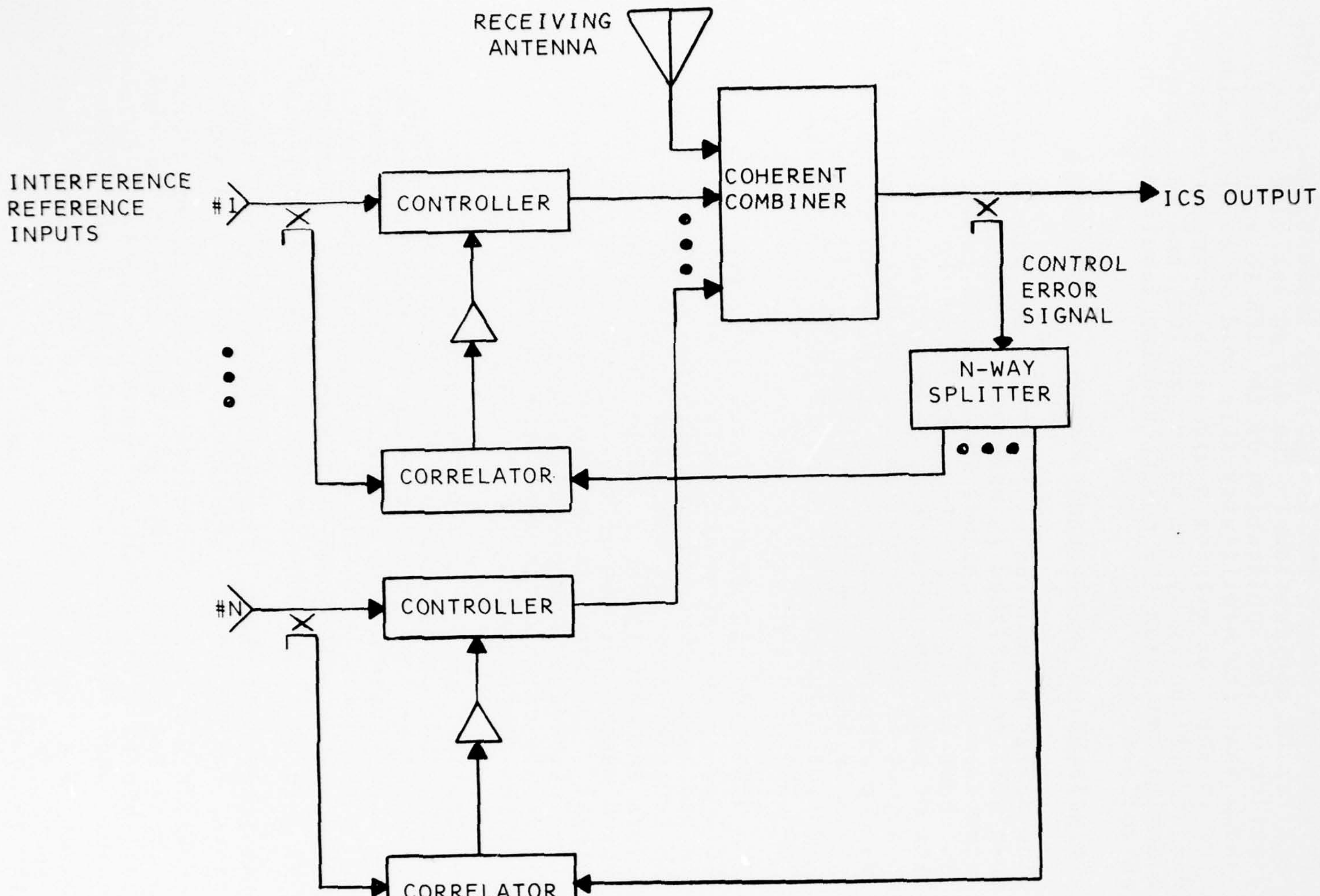


FIGURE 1 - ICS FUNCTIONAL BLOCK DIAGRAM

two quadrature components (I and Q), applying bipolar (plus/minus) adjustable attenuation independently to each component, and then combining the attenuator outputs in phase. A block diagram of such a controller is given in Figure 2.

1.3 SYSTEM ASPECTS

A study of high level interference cancellation inevitably leads to a study of the system in which it will be used. At HF and below, high power transmission is required to overcome space loss but also to exceed the ambient noise level at the receiver site. The ambient noise level varies with location and time of day (CCIR Report 322, 10th Plenary Assembly. *Reference Data for Radio Engineers* (Howard W. Sams, Sixth Edition, page 29-3) summarizes these data. The atmospheric noise level varies from 150 to 175 dB above kTB at 10 kHz, from 75 to 140 dB above kTB at 100 kHz and from 10 to 90 dB above kTB at 1 MHz. Including man-made noise (quiet location) and galactic noise with atmospheric noise, the levels vary from 40 to 60 dB above kTB at 3 MHz and drop to about 20 dB above kTB at 30 MHz. This is afternoon data. At nighttime, when propagation improves, the ambient noise level rises considerably.

From the standpoint of reception, the implication is that the ambient noise level, signal and interference may all be attenuated to the point where the ambient noise level approximates the receiver equivalent input noise level before the signal-to-noise ratio is degraded by 3 dB. Attenuating the interference level prior to subjecting the combined signal to receiver processes reduces the degradation due to intermodulation and harmonic generation. For this reason, most receivers designed for operation in the presence of high level interferences control gain by means of switched attenuators which precede potentially nonlinear devices.

Since electronic interference cancellers utilize devices in which the RF and control signals interact, cancellation should take place at the lowest possible power level.

At the lower frequencies the signal plus noise plus interference can be attenuated drastically without significantly affecting the signal-to-noise ratio because the ambient noise power far exceeds the receiver's front end noise power. At 30 MHz, it would appear that the amount of attenuation permitted is minimal, unless high level interfering signals are present.

A single loop interference canceller will attenuate one interfering signal. The cancellation bandwidth is a function of implementation. In general, it will be sufficiently wide to attenuate close-in white noise from a transmitter as well as the transmitted signal and its sidebands.

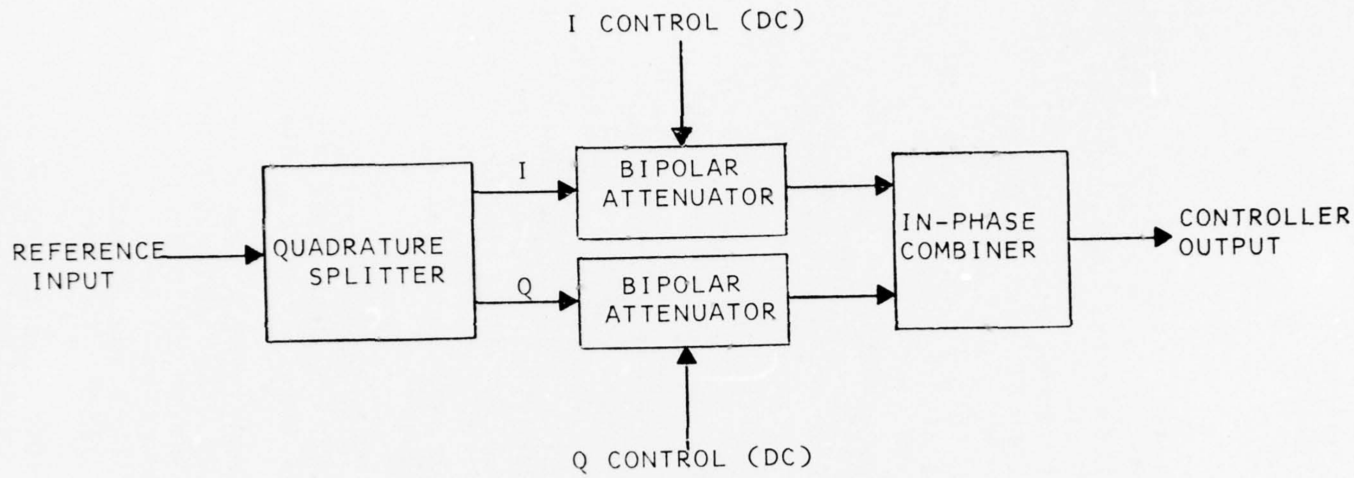


FIGURE 2

FUNCTIONAL BLOCK DIAGRAM OF I&Q CONTROLLER

The interference canceller permits the reception of signals at frequency separations which would be impractical with filter implementations. In particular, it permits the reception of a weak signal in the face of an interfering signal lying inside the receiver RF passband and outside the receiver IF passband when the ratio of the two signal levels at the receive antenna is well beyond the capability of the unaided receiver.

Since the single loop interference canceller does not cancel perfectly nor does it cancel transmitter harmonics, the uncancelled residue must be considered as relatively high level interference from the standpoint of the receiver. Therefore, even at the high end of the band, attenuation following the receive antenna can improve receiver performance provided such attenuation results in a corresponding improvement in interference cancellation.

The concept of deliberately introducing attenuation ahead of a receiver is admittedly difficult to accept. It is for this reason that the concept is introduced early in this report.

The breadboard phase of this program establishes state-of-the-art limits for a dual channel all-electronic HF interference canceller. It also points the way to the design of an optimal system to fit a given set of parameters. It is so designed that its performance may be optimized for those parameters without major redesign.

Table 1 summarizes the performance achieved by the experimental HFICS under this program.

TABLE 1

PERFORMANCE SUMMARY

DUAL-CHANNEL HIGH POWER HF ICS
(Breadboard)

Design Parameters

Max Transmitter Power per Channel	+62 dBm 1600 watts
Max Interference Level at Receive Antenna per Channel	+47 dBm 50 watts
Max Interference Level of Receive Antenna Dual Channel (PEP)	+53 dBm 200 watts
Insertion Loss - Each Transmitter	1 dB
Insertion Loss - Receiver	7 dB

Performance Data

Nominal Cancellation Ratio	
Dual Channel (4.5)*	28 to 50 dB
One Channel CW (4.7)	47 to 53 dB
One Channel Two Tone (4.7)	28 to 43 dB
Acquisition Time (4.4)	2 ms max
Weight (4.8)	115 pounds
Power - 110 volts 60 Hz (4.10)	517 watts
Size: Width	20-1/4"
Depth	14-1/2"
Height	22-3/4"

*() is section reference.

SECTION 2 - HIGH POWER INTERFERENCE CANCELLATION

2.1 DUAL-CHANNEL HFICS - OVERVIEW

The dual-channel HFICS is designed to cancel relatively high level interfering signals from two colocated transmitters. The interfering signals are reduced to a level which will permit receivers to operate without damage and to tune to frequencies much closer to the transmitted frequencies than would be possible with conventional filtering techniques.

The dual-channel HFICS does not permit normal reception at the harmonics of the transmitters or at frequencies falling on intermodulation products thereof. This restriction also applies to filter techniques, because intermodulation products and harmonics are also generated within HF transmitters.

Figure 3 outlines the insertion loss of the various elements of the dual-channel HFICS. The reference signal tap from the transmitter reduces the available transmitter power 1 dB. The reference signal level is 7 dB below the transmitter power level.

The transmitter-to-receiver antenna coupling is assumed to be near-field with a space loss as low as 14 dB. There is 1 dB splitting loss in the ICS reference samplers. The signal from a +60 dBm transmitter is +45 dBm entering the receive antenna. With two transmitters, the signal is +51 dBm PEP at this point (+53 dBm or 200W PEP worst-case). Obviously, protection is required for the receiver.

The protection may be in the form of filtering, limiting, attenuation and/or interference cancellation. If the frequencies are closely spaced, filtering is impractical. The choice, then, lies between attenuation, limiting and interference cancellation. If burn-out protection alone is required, a limiter would undoubtedly be the best choice. However, limiters decrease the desired signal-to-interference ratio and introduce new spurious signals.

HF receivers are nonlinear devices. There is a limit to the absolute magnitude of the interference level before the sensitivity threshold degrades. With electromechanical tuning, this limit increases rapidly with desired signal-to-interference separation. In the more modern all-electronic receivers (incorporating band switched or varactor tuned RF filters), this is no longer true. Attenuators decrease interference, transmitter broadband noise, and the desired signal equally. The desired signal-to-interference ratio is unchanged.

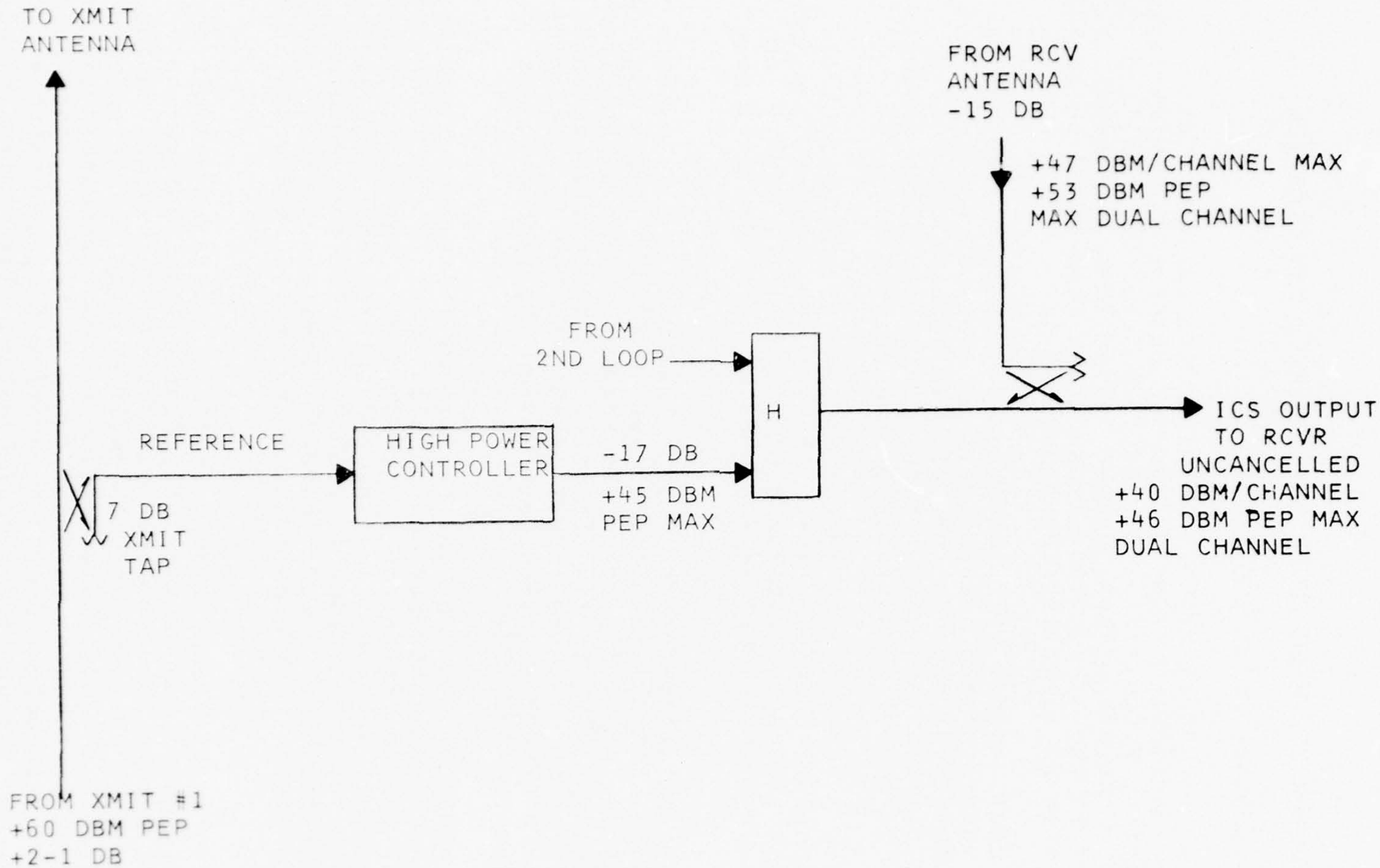


FIGURE 3

HFICS - MINIMUM INSERTION LOSS DIAGRAM

The interference canceller cancels the interfering signal and to a lesser extent, the broadband noise without affecting the desired signal. The insertion loss introduced by the ICS attenuates the entire antenna signal equally. The desired signal-to-interference and broadband noise ratios are increased by their respective interference cancellation ratios.

An interference canceller samples the interfering signal, modulates it in phase and amplitude so that when that sample is combined with the received signal, the interference residue is minimized. Referring again to Figure 3, the receiving antenna feeds the through port of a 7 dB directional coupler. The output of the through port is terminated.

The maximum interference signal level per channel is +47 dBm (+62 dBm transmitter). This signal splits between the two output ports of the directional coupler. The signal into the load is down 1 dB due to the splitting loss or +46 dBm/channel maximum. The uncancelled signal to the receiver is down 7 dB or +40 dBm/channel maximum.

In order to cancel the interference, the reference signal at the output of the 7 dB coupler must equal the interference level. At the reference input to the 7 dB coupler, it must be 1 dB higher to allow for splitting losses. Another 3 dB splitting loss occurs in the dual channel combining hybrid. Allowing 1 dB for the insertion loss of the two devices, the weighted reference signal out of the high power controller must be 5 dB higher than the uncancelled interference level at the receiver port.

The high power control (complex weight) introduces a minimum loss of 10 dB at 0°, 90°, 180° and 270° phase shifts. The coupling factor of the transmitter tap is 7 dB. As can be seen in Figure 3, these losses reduce each controller's RF level to +40 dBm PEP at the ICS output.

2.2 HIGH POWER CONTROLLER

The high power controller is essentially an amplitude and phase modulator. It may be implemented in many ways. The simplest in concept is to split the signal into four channels separated by 90° phase increments, control the gain or loss in each channel, and then recombine the four signals. The resultant can be controlled in phase and amplitude by amplitude modulating each channel. The 90° phase increments may be accomplished by means of an all-pass network over relatively wide bands. The high level amplitude control is the more difficult problem.

The amplitude controls, to be of use in a feedback system, should be monotonic, should have maximum isolation between the low frequency control signal and the RF signal and should introduce minimal distortion or noise into the RF signal path.

Electronically variable elements fall into four categories: capacitors, inductors, resistors and amplifiers. Electronically variable capacitors have proven practical for low power level tuning elements. When the RF signal becomes large with respect to the control signal, the capacitance variation becomes RF dependent. In this application, the signal level at the output of the amplitude modulator may reach +44 dBm (25 watts).

The electronically variable capacitor is essentially a reverse-biased diode with a relatively large junction capacity. The junction capacity varies with control voltage. Since it also varies with signal voltage, it is not well-suited for the control of the power levels encountered in this application.

Electronically variable inductors are somewhat more feasible than voltage variable capacitors. They have proven practical in relatively high power tuned circuits and antenna matching networks. These devices come under the general heading of saturable reactors. It is possible to provide appreciable isolation between the control and controlled waveforms.

The devices depend on the change in magnetic permeability of a magnetic (ferrite) material with magnetic flux level. Since the flux level is not independent of the RF field, some RF distortion is to be expected. This is especially true if the core material is operated close to saturation. This latter problem can be averted by using relatively large ferrite cores.

Saturating large ferrite cores requires large amounts of flux. The high power saturable reactor control systems implemented to date have been essentially step function systems. In many cases, a return to zero implementation has been used in order to cope with the hysteresis inherent in high permeability magnetic systems. For a high power controller, a linear control system capable of coping with hysteresis in the control loop would have to be designed.

The saturable reactor approach appears particularly attractive for VLF and LF where the response time can be relatively long. The hysteresis problem together with the sparsity of available distortion data makes the saturable reactor a high risk approach at HF.

A gain-controlled amplifier is another candidate. The power required out of the amplifier is +47 dBm PEP (50 watts). (At the time the system study was initiated, the levels were 3 dB higher or 100 watts.) A typical tube for this application

(8122) will introduce third-order distortion products 34 dB down under the most favorable conditions. These distortion products place a floor on the cancellation available since they differ from the signal being cancelled.

The vacuum tube amplifier approach introduces several other very serious considerations. The output impedance of the tube is high. Either an essentially narrowband tuned matching circuit is required or a distributed amplifier approach is required. The tuned circuit implies electromechanical tuning, the distributed amplifier implies a multiplicity of tubes and is costly. Amplifiers, in general, introduce noise into the cancellation residue which cannot be bandlimited without electromechanical tuning.

Vacuum tubes are available with two grids, permitting isolation between the gain control and the signal input. High level transistor amplifiers do not presently have this degree of freedom.

Transistor amplifiers do not present the bandwidth limitation inherent with vacuum tubes. The distortion problem is on a par with tubes. However, they can be readily parallelled to alleviate this situation. Gain control must be instituted by low level attenuation ahead of the amplifier.

Such a combination is possible. However, the efficiency and weight of commercially available amplifiers makes this approach unattractive.

The ENI A-300 amplifier has a third-order intercept of +64 dBm. It weighs 88 pounds and consumes 2 kilowatts of power. Such an amplifier could function for both channels in a dual channel ICS system. With both channels cancelling CW signals, the amplifier would be subjected to a two-tone +39 dBm signal (+45 dBm PEP). This signal would generate third-order distortion products 50 dB down worst-case.

Such a system is intriguing. Its use would relax the distortion requirement on the system modulators but would degrade the receiver noise figure. The amount of degradation is dependent on the gain required to permit the development of a suitable modulator. Moreover, as will be shown later, system noise figure becomes less important with decreasing frequency. At HF, a considerable degradation in the signal-to-noise ratio is permissible at the receiver input because of the high ambient noise level.

The low level modulator/amplifier approach does not meet the original design goals from the standpoint of power consumption, additive noise and cancellation residue. It also pushes the weight goal. It does relax the modulator requirement.

The electron-bombarded semiconductor (EBS) is a device which may prove useful in future developments.* The device can be broadbanded, will handle high power and has excellent isolation between the control and controlled circuits. At the time this program was initiated, the EBS had been reduced to practice for a few specialized purposes. It was considered to be too high a technical risk to pursue until more conventional approaches were exhausted.

The preceding survey covers the present state of the high level, all-electronic modulation field with the exception of the PIN diode.

2.3 PIN DIODE ATTENUATORS

The PIN diode has had wide acceptance as a means of RF switching and RF attenuation. It is a two-terminal device. Isolation between the RF signal and the control signal is predicated on stored charge in the intrinsic layer of the diode.

The control signal stores charge in this layer. The RF signal alternately increases and diminishes the charge. When the RF frequency is high, relatively little charge is removed before the cycle is reversed. As a result, the conductivity remains essentially constant and the RF signal is undistorted. As the frequency decreases, the amount of charge change per half cycle increases and the distortion increases.

The distortion may be reduced by increasing the ratio of control current to RF current at the desired attenuation level. However, the RF resistance of the PIN diode decreases as control current increases. This implies an impedance transformation to an impedance consistent with the diode resistance range.

Operation in the HF range limits the choice of PIN diodes to those with relatively long carrier lifetimes if the stored charge is to be relatively constant over a half-cycle. The 50-watt attenuator output also implies that, under some operating conditions, the PIN diodes in the attenuator will have to absorb 50 watts in addition to other losses. High power PIN diodes are required.

At this time, the sole source for such diodes is the Unitrode Corporation of Watertown, MA. Their UM4301 diode comes closest to meeting the attenuator requirements. The device can dissipate six watts when heat-sunk to +125°C. It has a carrier lifetime of 5 microseconds and a resistance of 1.5 ohms at 100 mA or 0.1 ohm at 1.5 amperes of control current. It is not an ideal device for the application, but it is the best available.

*W&J Technical Notes, vol. 3, no. 1, Jan/Feb 1976.

From strictly a thermal standpoint it is necessary to use a multiplicity of diodes. From a distortion standpoint, it is desirable to use as many diodes as possible in order to keep the ratio of RF-to-control current as low as possible. As will be seen in the discussion of the bipolar attenuator, a compromise must be made in establishing the number of diodes based on considerations of heat dissipation, distortion, operating bandwidth, minimum insertion loss, and cost.

In general, the use of more diodes per bipolar attenuator permits higher operating power levels with less distortion. However, the use of more diodes increases the minimum insertion loss (thus requiring more reference power), introduces more difficulty in obtaining the required bandwidth, and increases the cost.

The present design uses 16 diodes per bipolar attenuator or 64 diodes per dual-channel HFICS.

It is understood that Unitrode is developing high power PIN diodes with extended I regions. This construction should result in greater stored charge per diode which, in turn, should result in lower distortion. It may permit operating with fewer diodes, which should simplify the attenuator design.

Section 3 covers the elements of the dual channel HFICS designed around high power controllers in which PIN diodes form the means of attenuation.

SECTION 3 - HFICS BREADBOARD DESIGN

The HFICS is a dual-channel interference cancellation system designed to cancel signals from two 1 kW transmitters received on an antenna with 14 dB of Tx/Rx spatial isolation. Each transmitted signal is sampled by means of a 7 dB directional coupler. Each sample has its inphase and quadrature components weighted by a high power controller. The two conditioned reference signals are summed together and then subtracted from the received signal. A sample of the final output is fed back through control loops which set the high powered controllers to minimize the interference residue from the two transmitters at the receiver port. (See Figure 4.)

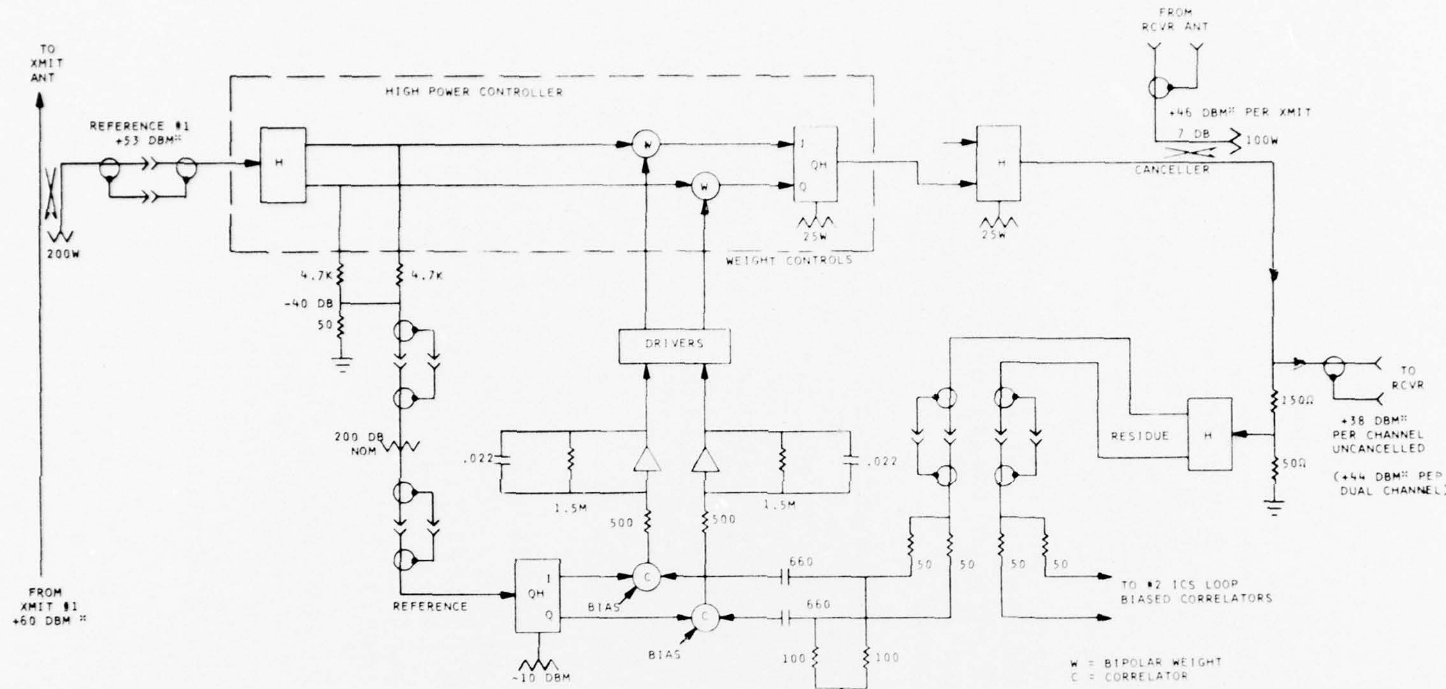
The high power controller consists of an inphase signal splitter (H), two bipolar attenuators (W) and a quadrature combined (QH). The minimum insertion loss of such a controller varies with phase shift. In the following discussion, lossless elements are assumed.

Each bipolar attenuator can amplitude modulate the signal and invert its sum. The 0° reference is taken with the in-phase bipolar attenuator set for minimum (noninverted) attenuation and the quadrature attenuator set for maximum attenuation. With lossless components, the insertion loss for the controller would be 6 dB at 0°, 90°, 180° and 270°, decreasing to 3 dB at 45°, 135°, 225° and 315°. In practice, the minimum insertion loss over the HF band at 0°, 90°, 180° and 270° may be as high as 10 dB. This figure is used as a design parameter in determining the maximum usable ratio of interfering signal power-to-reference power.

The outputs of the two high powered controllers are summed in an inphase combiner. The summed signal is then combined with the signal from the receiving antenna by means of a 7 dB directional coupler. Cancellation of the interfering signals takes place in this coupler. The signal from the receiving antenna is attenuated 7 dB in the coupler.

A resistive tap samples the signal to the receiver after cancellation. Prior to cancellation, the interference may be as high as 25 watts PEP at the receiver input. The sampled residue is fed to an inphase hybrid splitter, and is further divided and fed to inphase and quadrature correlators by means of resistive splitters.

The reference for the correlators is taken from the high power controller by means of a resistive divider. The initial resistive divider provides 40 dB of attenuation. An additional 20 dB of attenuation is supplied by means of in-line attenuators. These attenuators may be changed to modify the reference level



*+2-1 DB PEP

FIGURE 4

HFICS

SIMPLIFIED BLOCK DIAGRAM

when the system is to be used with lower power transmitters. The design power level at the input to the quadrature hybrid is -10 dBm, although this level is not critical. The system can tolerate levels as high as +30 dBm at this point without damage; however, cancellation may be degraded.

The two correlator outputs are lowpass filtered to extract the control signals and amplified to the level required for the drivers. The drivers, in turn, shape the control signals to properly set the bipolar attenuators and close the control loop.

3.1 BIPOLAR ATTENUATOR (Figure 5)

The heart of the high power controller is two pin diode bipolar attenuators. With nominal transmitter power, each attenuator must be capable of dissipating 100 watts (158 watts with maximum transmitter power). The signal to the attenuator is transformed from 50 ohms unbalanced to 3.13 ohms balanced by means of a 4:1 stepdown transformer. The balanced line is connected to similar step-up transformers through two diode attenuators connected in phase opposition.

The pin diode attenuators act as variable resistors whose resistance is DC current dependent. When the control currents are equal, the output signal approaches zero. The phase of the output signal is the insertion phase of the attenuator when the inphase (0°) diode string has the higher DC current. The phase reverses 180° when the 180° diode string has the higher DC current.

The driver circuits are designed to maintain that current in both legs which will result in the optimum compromise between a matched system and minimum distortion over the attenuation range.

The eight 0.1 μF blocking capacitors isolate the DC current from the output transformer. Embedding the pin diodes in a low impedance balanced line presents a bandwidth problem. Leakage inductance in the transformers and lead inductance in the diode connections will severely limit the bandwidth of the attenuator unless special precautions are taken.

The photograph of Figure 6 shows the attenuator design. Leadless pin diodes are soldered to copper rivets. The rivet transfers the heat generated by the diodes through a thermally conductive insulator (Chotherm 1661) to the heatsink.

The transformers consist of two tubes with one end joined to form a single turn. Six ferrite beads on the outside of each tube complete the magnetic circuit. Four turns of wire through the tube form the 50-ohm unbalanced winding.

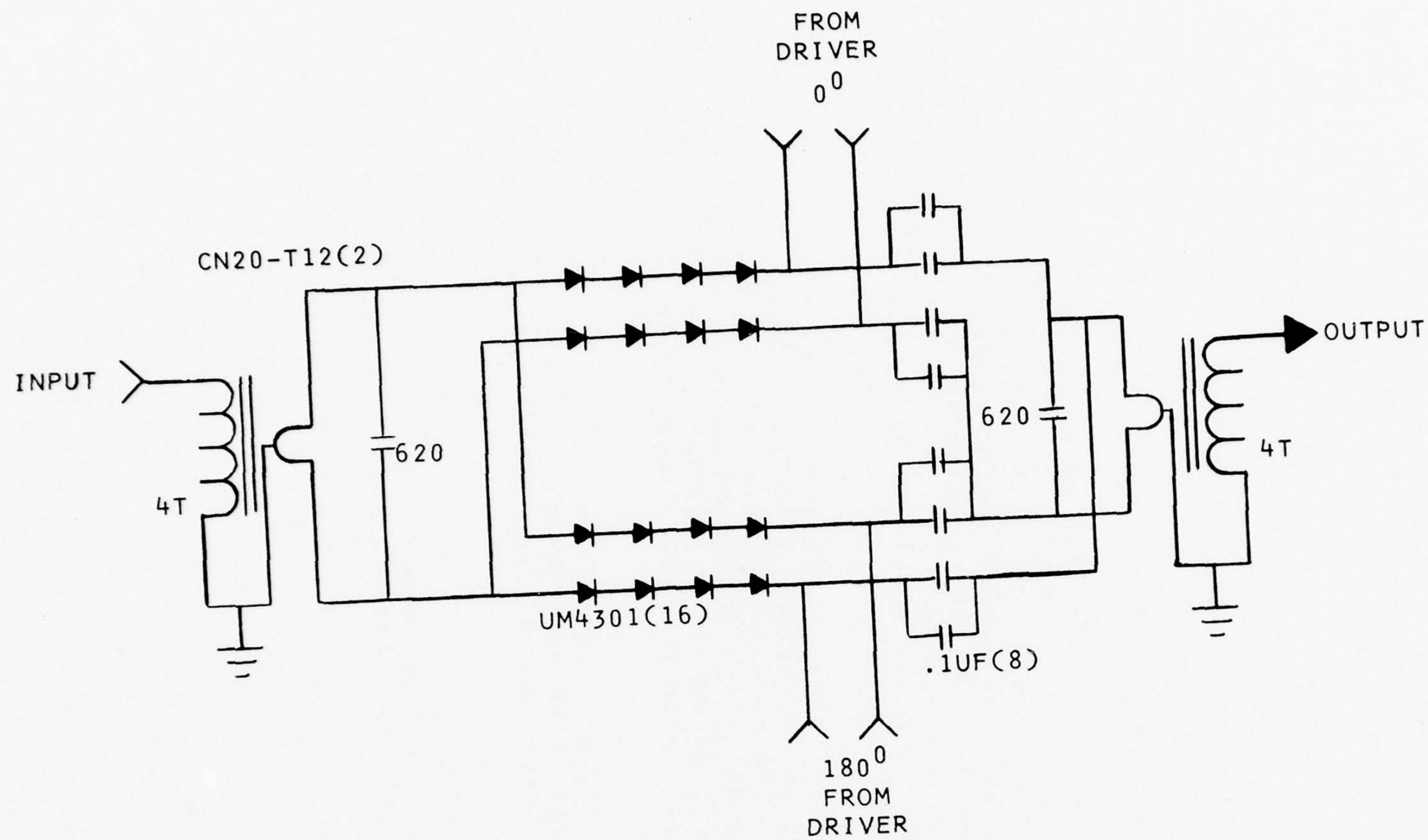


FIGURE 5

BIPOLAR PIN DIODE ATTENUATOR

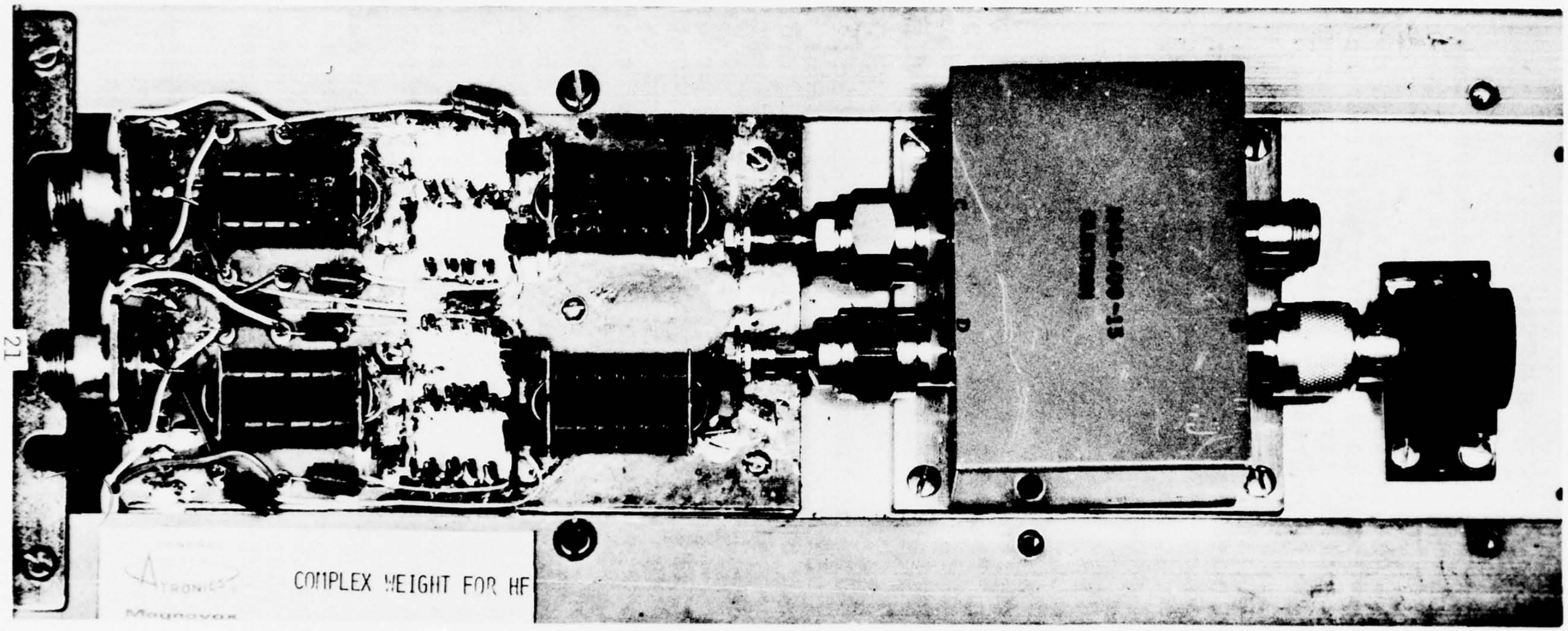


FIGURE 6
HIGH POWER CONTROLLER

The photograph also shows the quadrature combiner together with its loads and the ferrite chokes in the drive circuits.

At the time the photograph was taken, each diode was shunted with a resistor to insure even distribution of the signal at high attenuation levels. This proved unnecessary and these resistors were removed.

After taking all possible precautions to minimize inductance consistent with removing heat, bandwidth remained a problem. To solve the problem, the balanced line was treated as a filter. The two 620 pF capacitors convert the line into a lowpass filter with a cutoff at about 40 MHz.

3.2 DRIVERS

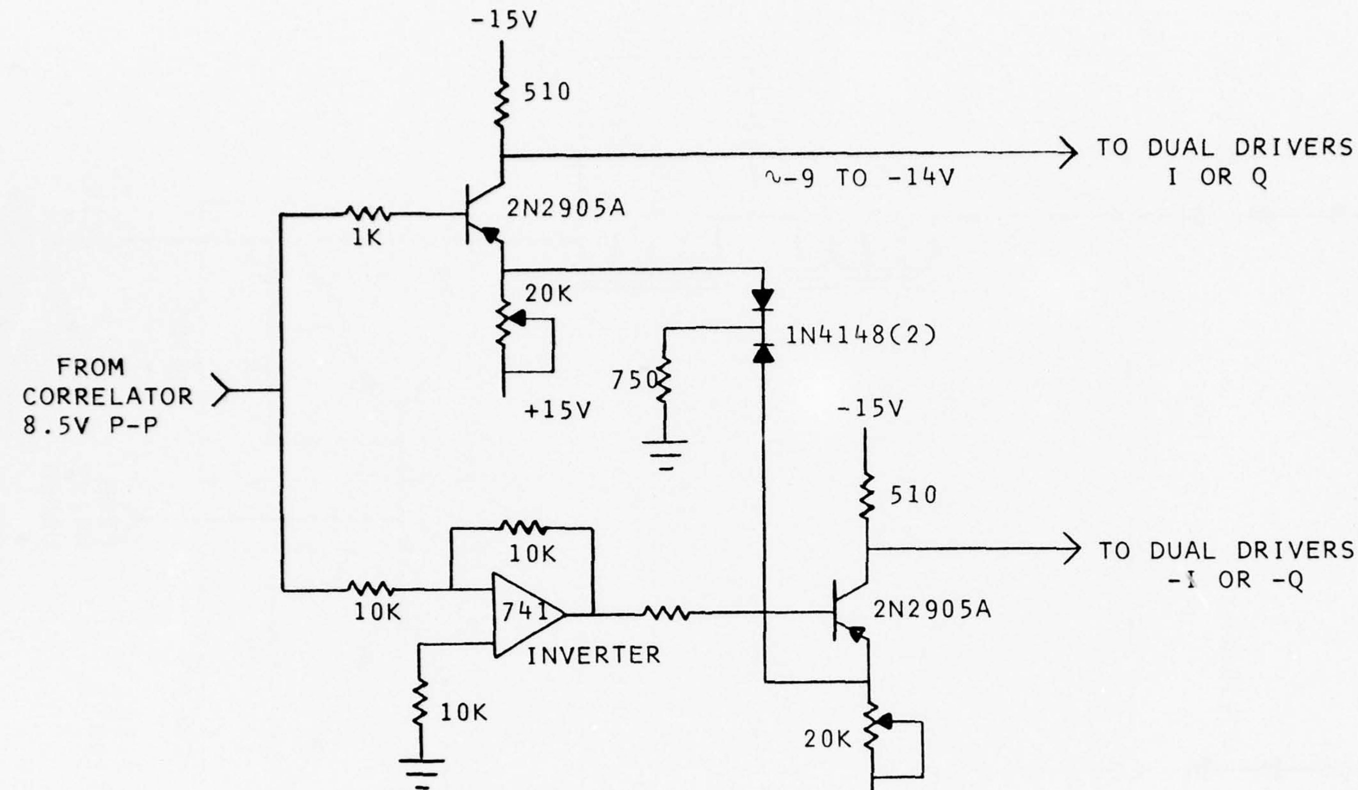
The bipolar attenuator driver is broken into two circuits, the drive shaper, Figure 7 and the dual drivers, Figure 8. The correlator output is a baseband signal at levels up to ± 8.5 volts. The drivers convert this signal to diode drive currents of up to 1.5 amperes.

In the bipolar attenuator, all diodes are energized. Attenuation is a maximum when the current in all diodes is equal. (The current level at maximum attenuation is the cross-over current.) Cross-over current occurs in the diode strings when the correlator output is at ground potential. The cross-over current is set to optimize the VSWR of the attenuator. At this point the resistance of eight diodes in series should equal 3.1 ohms or 0.39 ohm per diode. The current required is of the order of 0.4 ampere for the UM4301 diode to reach that resistance.

When the output of the correlator goes negative, the current through the "inphase" diodes increases and the current through the "reverse-phase" diodes decreases. The function is reversed when the correlator output goes positive. The drive current is shaped so that the attenuator VSWR is relatively independent of attenuation level and so that the attenuation varies approximately linearly with correlator output.

The drive shaper is shown in Figure 7. The output of the correlator is split into two paths. One path goes to the "inphase" shaper and the other goes through a unity gain inverter to the "inverse-phase" shaper. The shaper is a PNP transistor with a fixed collector resistor and a diode-switched emitter resistor.

When the base is at ground potential, the emitter resistor is a 20k potentiometer. The potentiometer is set so that the drop across the collector resistor is that required to drive the



SET POTS WITH INPUT GROUNDED
FOR 1.5V DROP ACROSS EMITTER
RESISTORS OF DUAL DRIVERS

FIGURE 7

DRIVER SHAPER FOR BIPOLAR ATTENUATOR

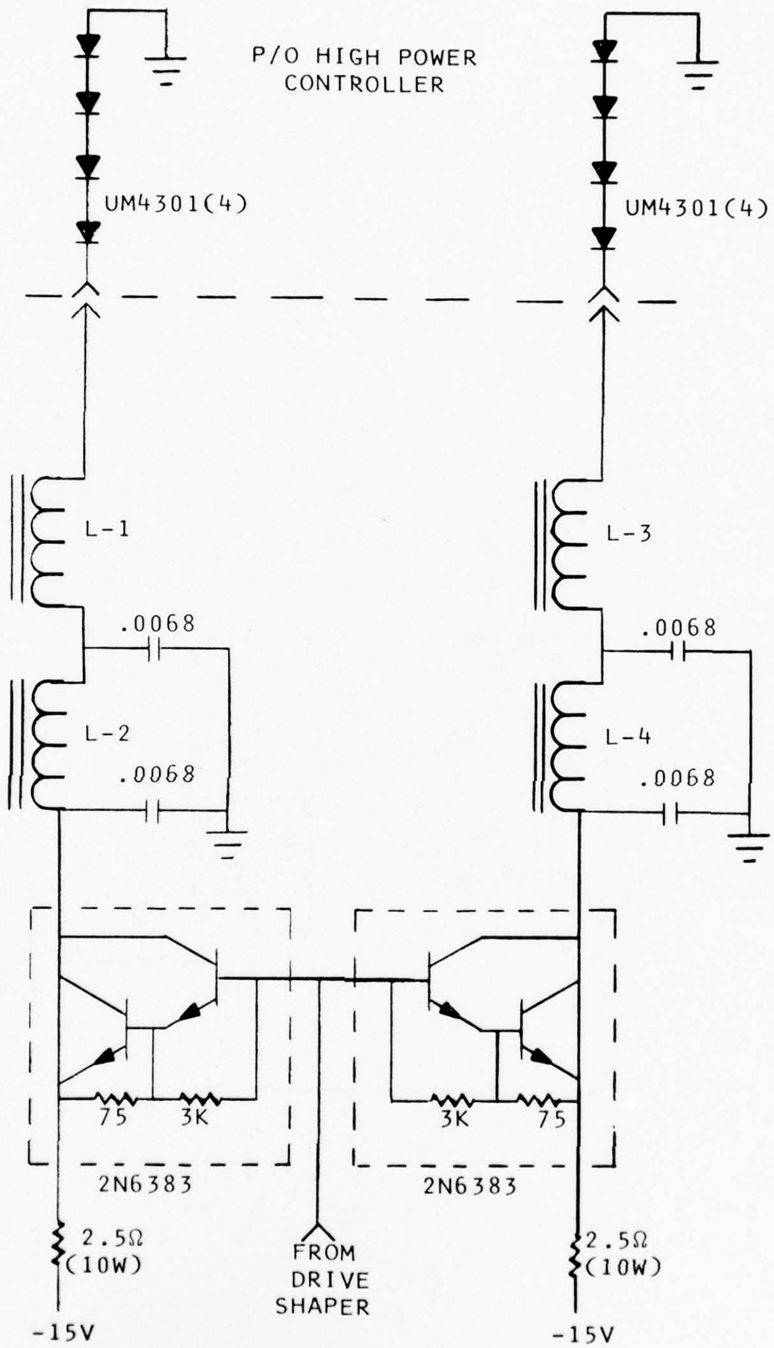


FIGURE 8
DUAL DRIVERS (TWO REQUIRED PER BIPOLAR ATTENUATOR)

dual drivers (Figure 8) to approximately 0.4 ampere (attenuator VSWR minimized).

This emitter resistor setting determines the drive shaper gain when the base is at ground potential or positive with respect to ground. When the base reaches two diode drops below ground, the 750-ohm resistor is diode switched in parallel with the 20k potentiometer. The gain of the amplifier increases because of the decrease in degeneration. This increase in gain is sufficient to linearize the system and to keep the reflected power of the high power controller below 7 dB over the entire operating range.

A dual driver, Figure 8, follows each driver shaper output. The dual driver consists of two Darlington transistors connected to act as voltage-to-current converters. The Darlington drives the diode strings in a balanced line in the High Power Controller. At maximum current (1.5 amp) the base-emitter drop is about 2 volts and the drop across the 2.5-ohm resistor is 3.75 volts. The drop across the four PIN diodes is about 4 volts, leaving a collector-to-emitter voltage of 5.25 volts across the Darlington transistor. This is more than ample to insure that the current through the diode string is virtually independent of minor variations in diode string drop. The lowpass filter consisting of ferrite loaded chokes and 0.0068 μF capacitors isolates the control circuit from the RF power in the bipolar attenuator.

3.3 CORRELATOR

The correlator is a synchronous detector which compares the cancelled residue (error waveform) with each quadrature component of the transmitter signal (reference). Figure 9 is a schematic of the correlator. The circuit is based on a single-balanced mixer. In a single-balanced mixer, the LO port is isolated by balance. The RF and IF ports are isolated by highpass and lowpass filters.

In this correlator the reference port feeds the balanced transformer. The error port (RF) is isolated from the product port (IF) by the two 330 pF capacitors and the product port is isolated from the error port by a lowpass active filter. The 0.0047 μF capacitor provides additional RF filtering for frequencies beyond the active filter response.

In the initial development phase, the correlator was hardlimited at the reference port. Hardlimiting the reference signal results in minimum correlation loss but also introduces high level odd harmonics in the reference. These harmonics correlate with similar harmonics in the error signal. The harmonic correlation places a floor on the cancellation of the fundamental signal.

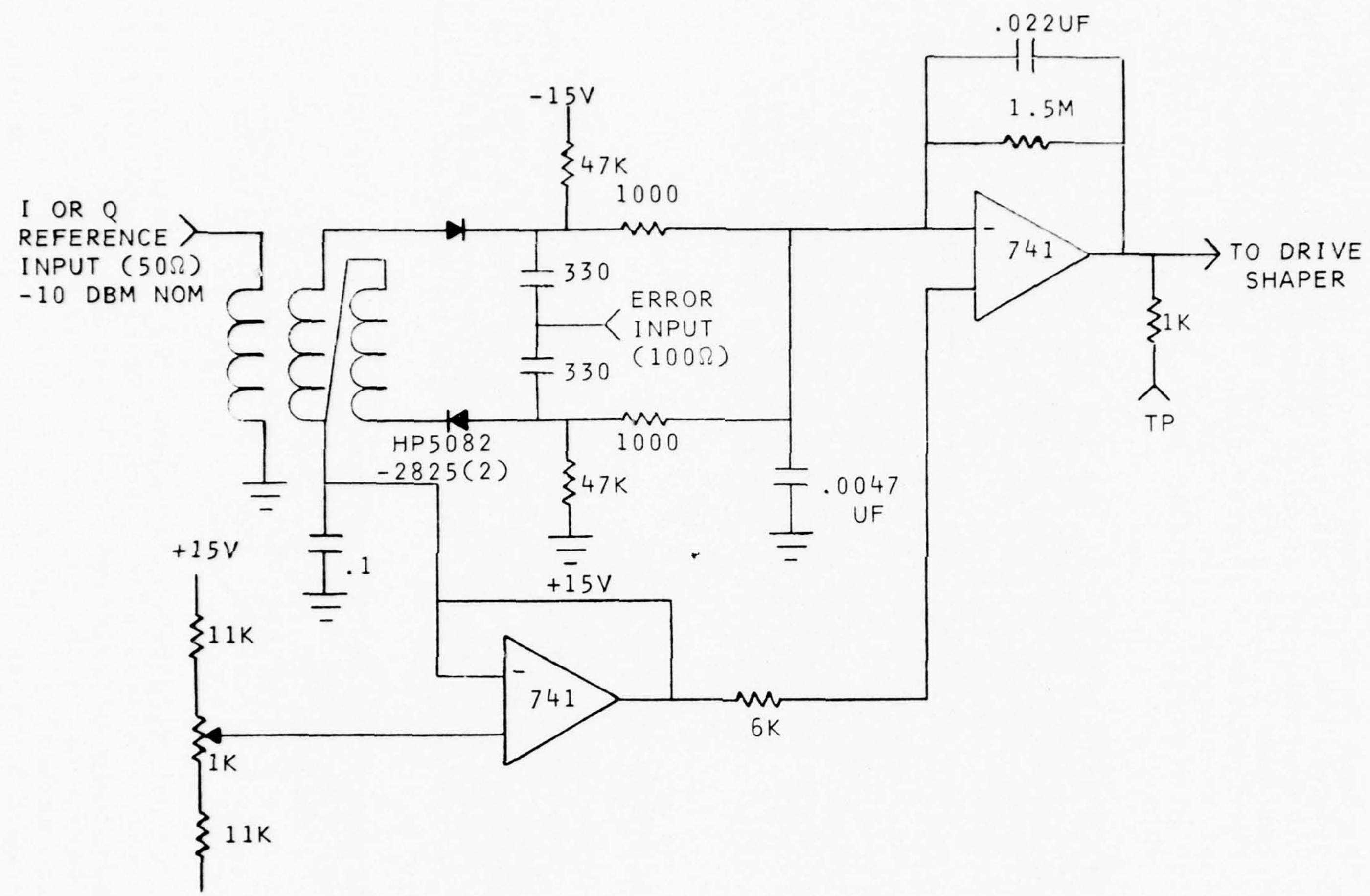


FIGURE 9
CORRELATOR (I OR Q)

The conversion loss of a mixer increases abruptly when the drive power is reduced below that required to switch the diode state. The loss can be minimized by biasing the diodes. The 47k resistors supply the diode current required to optimize sensitivity with a reference signal of -10 dBm.

The lowpass filter is a high gain (70 dB) DC amplifier. In order to minimize the effect of DC offsets introduced by power supply imbalance, advantage is taken of the common mode rejection afforded by the active circuit.

The center tap of the transformer is also the center tap of the diode bias string. This point is bypassed to ground through a 0.1 μF capacitor. An adjustable bias is connected through a voltage follower to the diode center tap and the noninverting input of the lowpass filter amplifier. Minor bias variations pass through the filter unamplified.

The adjustable bias permits adjusting the system DC offsets.* Offsets introduced by tracking error between the positive and negative supplies are minimized by common mode rejection.

3.4 POWER SUPPLY

Two DC power supplies are incorporated in the HFICS. One supply is a Teledynamics T12/15-750 dual output supply. This supply is set for ±16.5 volts. It is connected for series tracking. The supply is capable of furnishing 0.75 ampere in each leg. Ripple is less than 7.5 mV and regulation is better than 0.1% for both line and load. Under normal operating conditions, the supply is operating at less than 50% of its rating.

The high power supply is a Teledynamics BRUTE II with rippler reduction kit K2-11. This unit has 24-ampere capacity up to 24 volts. It normally operates at -17.5 volts. The maximum system current drain is 16 amperes (worst-case). This supply has an efficiency of greater than 75%. In order to achieve the efficiency, SCR control is used. The maximum ripple is 0.25 volt peak-to-peak. The high ripple voltage is removed by means of an active rippler filter (Figure 10). Four 2N6053 Darlington transistors are connected in parallel to form a series-pass transistor requiring a minimum collector emitter drop.

The base inputs of the four Darlingtons are connected through 150-ohm resistors to the well-regulated -16.5 volt output of the dual power supply. The four 150-ohm resistors serve to

*For a mathematical treatment of the effect of DC offsets upon a feedback cancellation loop, see: "Multiplier Offset Voltages in Adaptive Arrays," R. T. Compton, Jr., IEEE *Trans on AES*, September 1976, pp. 616-627.

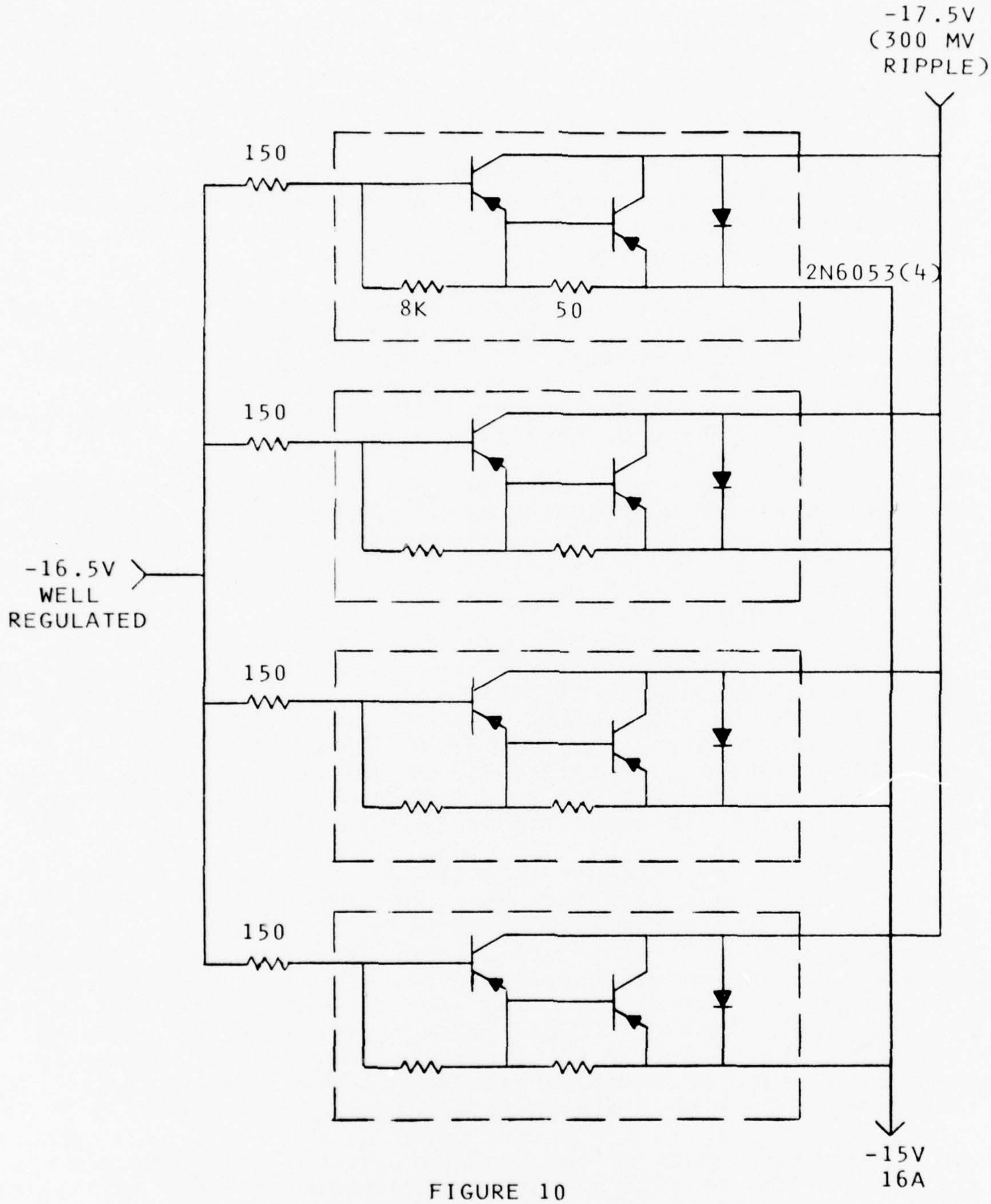


FIGURE 10

-15V SUPPLY RIPPLE FILTER

equalize the current distribution among the four Darlingtons. The filter effectively reduces the residual ripple to that of the dual supply or by a factor of ten.

SECTION 4 - HFICS TEST PROGRAM

4.1 INTRODUCTION

When an HF receiving antenna is operated in close proximity to an HF transmitting antenna, an appreciable portion of the transmitter power is coupled into the receiving antenna. If the transmitting and receiving signals are spaced more than 10% apart in frequency, adequate isolation can be achieved by conventional filter techniques. Closer spacing requires other means of isolation (interference cancellation).

The HFICS provides a means of selectively attenuating interfering transmitter signals to a much greater degree than the desired signal. Unfortunately, any distortion introduced by the interference canceller will limit its own performance. It should be noted that distortion products in the cancellation residue will occur at the same frequencies as those present in available transmitters. This complicates the evaluation of HFICS.

For example, two transmitters operated simultaneously will generate, in addition to their fundamental frequencies, a host of harmonic frequencies. To the extent that the transmitting antennas are coupled and the transmitter final amplifiers are nonlinear, a family of intermodulation products will also be generated. It has also been shown that these products can be generated by nonlinear materials within the transmitting antenna fields. In addition, the transmitters generate bandlimited noise. The bandlimiting is that provided by the transmitted final filter. The latter is often nonexistent or, at best, compromised for transmitter efficiency.

These factors are mentioned because they are of importance in evaluating the usefulness of the HFICS. The HFICS can be expected to improve reception in close proximity to either of two transmitted frequencies. It cannot be expected to permit reception at those freuqencies which are currently limited by transmitter harmonics, intermodulation products or noise.

It should be noted that while transmitter noise will be reduced close to the transmitted frequencies by the HFICS, at frequencies removed from the transmitter frequency the noise may be increased as much as 6 dB. As implemented, the interference at the HFICS output prior to cancellation may be strong enough to damage the input of the receiver. It is, therefore, essential that the HFICS adapt rapidly.

The following tests are designed to evaluate the ability of the HFICS to cancel signals from one or two transmitters. Tests are made with CW signals and two-tone signals. The adaption time of the system is measured. The weight, size, and power

consumption of the breadboard are recorded with the understanding that no attempt was made in this design to minimize these parameters. The dual-channel HFICS is an exploratory development model.

4.2 DESIGN GOAL VERIFICATION

The design goals are based on Table II of RADC PR N-5-5001. They have been modified to be consistent with two +60 dBm transmitters isolated a minimum of 14 dB from the receiving antenna. It was determined that current airborne transmitters are operated at a maximum of +60 dBm rather than +63 dBm PEP as originally indicated. The test signals are either SSB or CW, since AM is rarely used at HF. Test results with CW also apply to FSK or quantized frequency modulation.

4.3 TEST SETUP

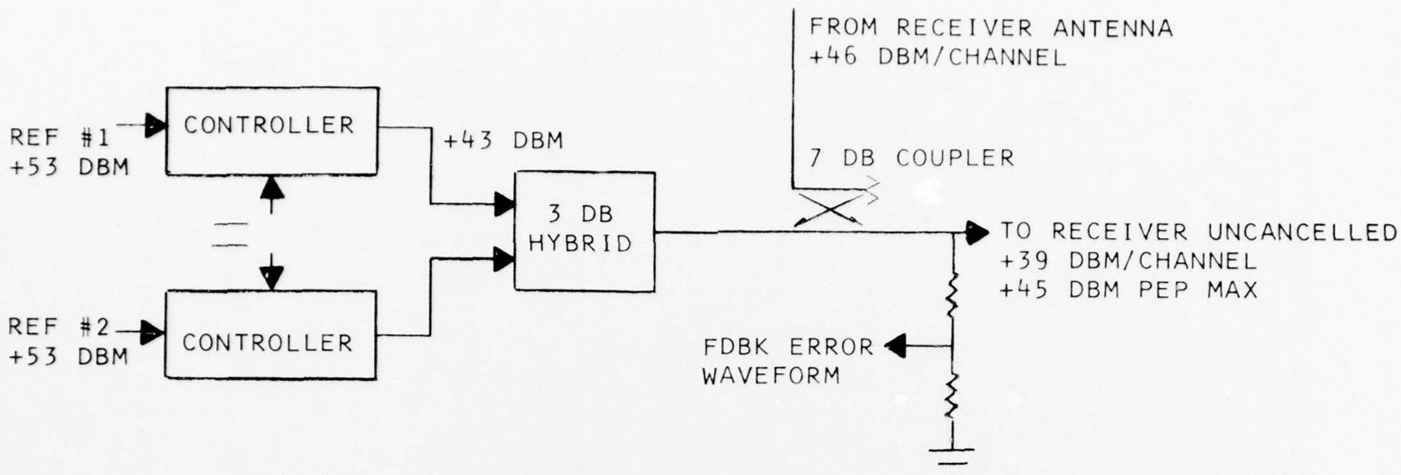
4.3.1 Test Setup - Single-Channel Modified (Figure 11)

The 7 dB transmitter directional coupler taps and the 7 dB receiver directional coupler are GFE items which are scheduled for delivery subsequent to the test date for the HFICS. In addition, the available test transmitters will not produce +60 dBm. Even at 400 watts, they must be operated on an intermittent basis to avoid self-damage.

Because of these limitations, certain modifications were made in the test circuit. These modifications do not change the normal operating levels of the HFICS. They do reduce the load on the test transmitters and permit operation with available 3 dB hybrids in lieu of the 7 dB hybrids.

Figure 11 shows the modifications to the HFICS. The upper diagram shows a portion of the block diagram of a two-channel HFICS. The two weighted transmitter references are combined in an hybrid. The combined weighted reference is subtracted from the receive signal. The residue goes to the receiver and also forms the ICS error signal. The insertion loss in the 3 dB high power coupler and in the 7 dB receiving hybrid are assumed to be 1 dB each for calculation purposes.

The modified block diagram for a single-channel test utilizes the 3 dB weighted reference combining hybrid to add the receiver antenna signal in lieu of the 7 dB coupler. The receive antenna signal in the single-channel modification is scaled down 3 dB from that in the dual-channel system. This figure is based on operating the weight (high power controller) at the same level in both systems.



DUAL-CHANNEL HFICS

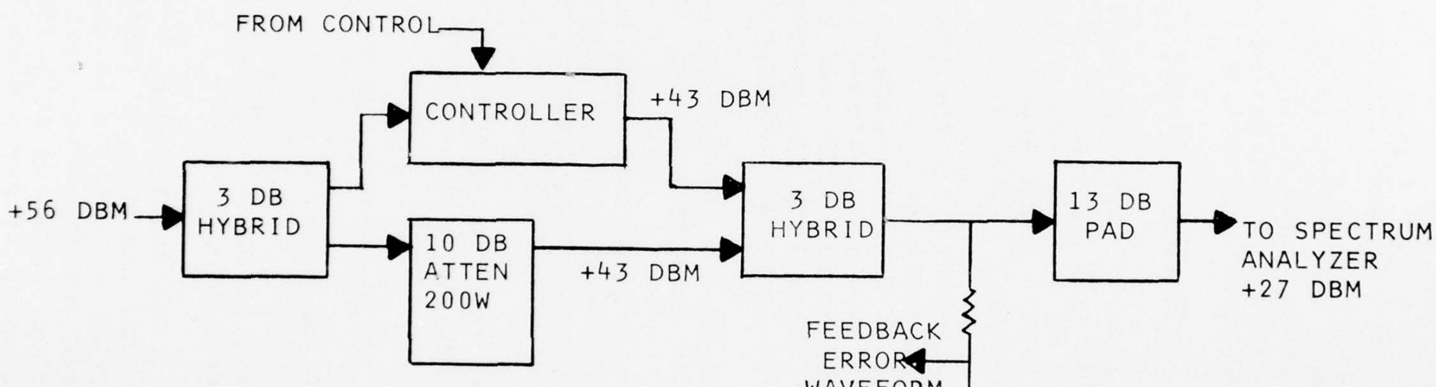


FIGURE 11

HFICS MODIFIED FOR TESTING SINGLE CHANNEL
AT DUAL CHANNEL LEVEL

The receiver output of the modified single channel HFICS is 11 dB below that of a dual channel HFICS with the same weighted reference signal. Thirteen dB is due to the attenuator and -2 dB to the modification.

Since distortion in the HFICS occurs primarily in the weight, tests based on the same weighted-reference-signal level are indicative of the performance to be expected when the 7 dB receiving antenna directional coupler becomes available.

4.3.2 Test Circuit - Single-Channel HFICS (Figure 12)

Figure 12 shows the modified single-channel HFICS in the test setup. As configured, the system can be operated with CW using one of the two audio generators to modulate the SSB transmitter or both audio generators to modulate the transmitter with a two-tone test signal for SSB operation.

The keyer turns the transmitter on and off by actuating the push-to-talk relay. The cycle is 14 seconds on, 10.5 seconds off. The on-time is adequate to obtain a reading but not long enough to permit the transmitter to reach its ultimate temperature. The on-off cycle reduces the power generated by 30%. This, together with the reduced power output generally used, is sufficient to prevent damage to the transmitter.

The CW key permits actuating the transmitter without relay chatter to measure acquisition time accurately.

The Bird 43 wattmeter permits measuring the forward and reflected power in the setup. Since most of the power feeds the HFICS, the VSWR measured is essentially that of the reference port of the HFICS.

The receiver output of the modified HFICS feeds a Tektronix 7L12 spectrum analyzer in lieu of a receiver.

4.4 ACQUISITION NULLING TEST TIME

4.4.1 Design Goal

No greater than 20 milliseconds after the interfering transmitter is energized.

The equipment is set up in accordance with Section 4.2.2. The spectrum analyzer is tuned to the transmitter frequency. The analyzer resolution is set to 3 kHz to simulate an SSB receiver and the frequency span is set for time domain operation. Single-shot operation is selected with the sensitivity set so that the scope triggers when the transmitter turns on. The scope

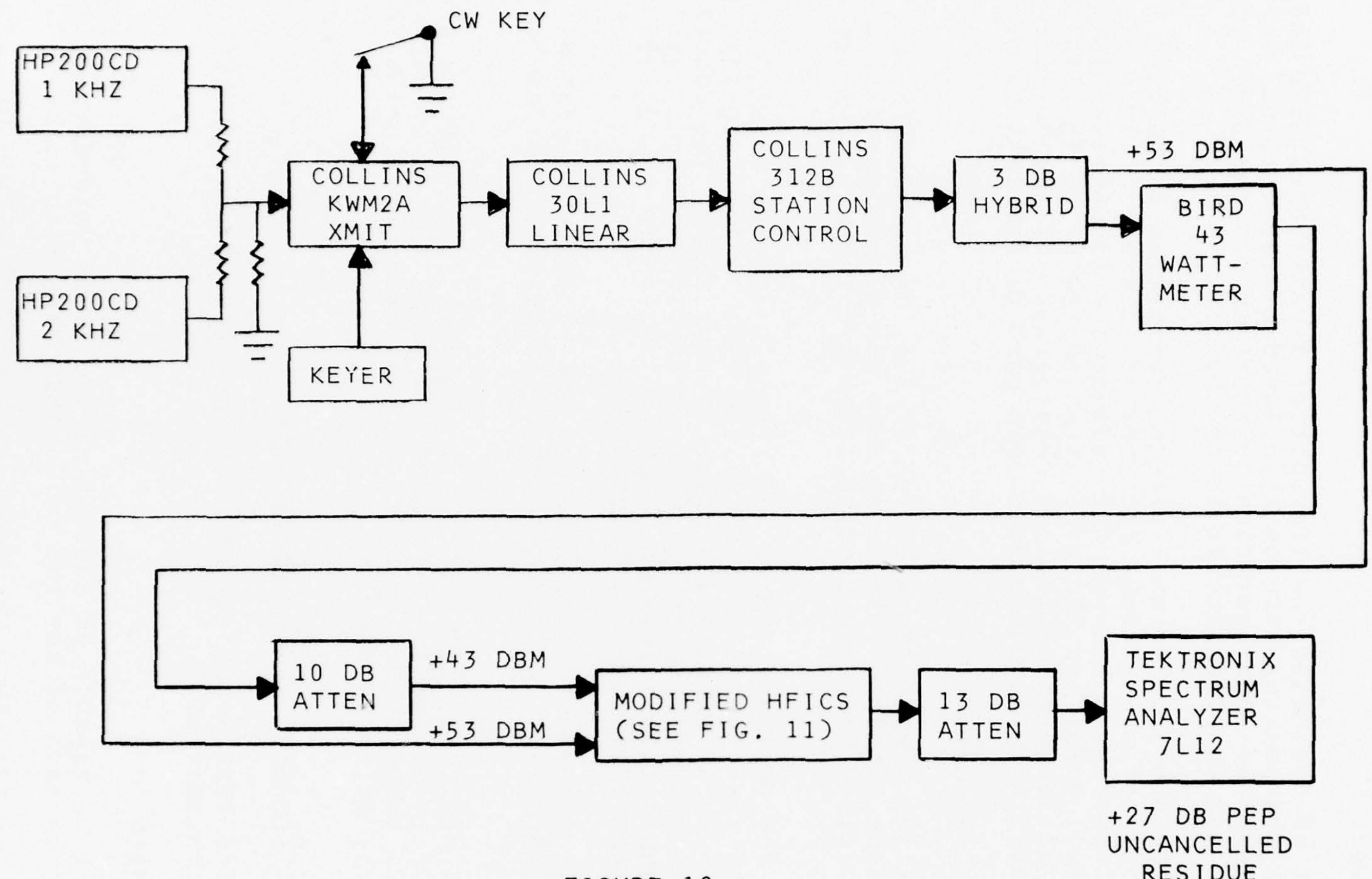


FIGURE 12

TEST SETUP - SINGLE-CHANNEL HFICS
(DUAL CHANNEL TEST LEVEL)

sweep is set for 2 milliseconds per division. The trace is set for storage.

For CW operation the transmitter is activated with the CW key. The transmitter turn-on is delayed by the internal keying filter. For two-tone operation, a short across the audio input is opened and the transmitter is on the air.

While there is no well-defined definition of nulling time, for purposes of measurement accuracy it is arbitrarily defined as the elapsed time between the instant the transmitter is within 1 dB of full power and the time at which the HFICS is within 10 dB of ultimate cancellation. Photographs of the nulling time with several modulation formats form part of the test report.

4.4.2 Test Results

Nulling time tests were run at 3.6, 14 and 21 MHz with CW and two-tone signals. All tests were run at maximum levels. The uncancelled and cancelled residues are taken on two sequential runs.

In the CW tests, where the transmitter took about 4 milliseconds to rise to within 1 dB of the final value, acquisition was within 10 dB of ultimate prior to that time. The cancellation residue rose to within 6 dB of the interference level before acquisition initiated. Interferences are cancelled by 20 dB in approximately 2 milliseconds.

With the two-tone test, there was no delay in transmitter turn-on. Acquisition took less than one millisecond for both tests.

The photographs of Figures 13 through 18 illustrate the results of these tests. The upper and lower traces of each photo represent, respectively, the ICS output power level prior to and immediately after turning the ICS on.

4.5 DUAL-CHANNEL CANCELLATION TEST

HFICS test setup for dual-channel operation with two colocated transmitters.

4.5.1 Design Goal

Must be capable of cancelling a maximum interference of +46 dBm from each of the two colocated transmitters.

Figure 19A shows the dual channel HFICS with 7 dB insertion loss between the receiving antenna and the receiver.

ICS OUTPUT:
NULLING TIME TEST
(Para. 4.4.2)

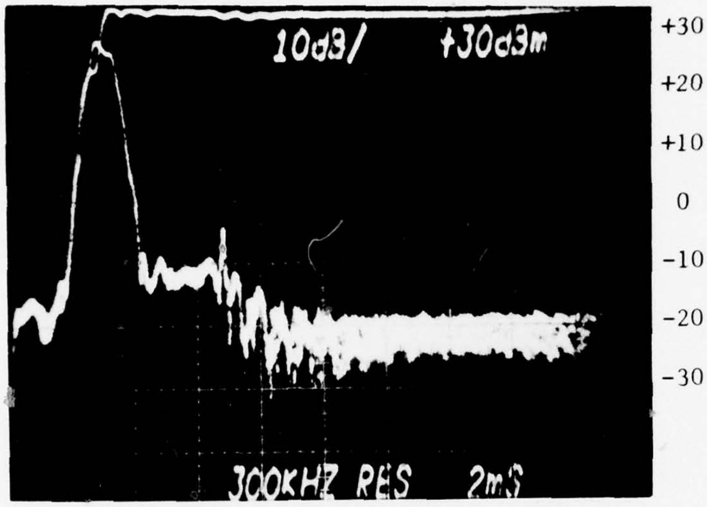


FIGURE 13

f = 3.6 MHz
MOD CW

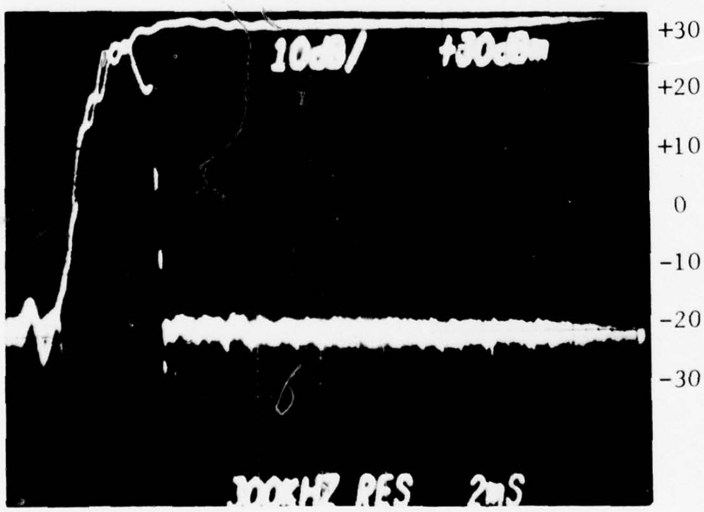


FIGURE 14

f = 14 MHz
MOD CW

ICS OUTPUT:
NULLING TIME TEST
(Para. 4.4.2)

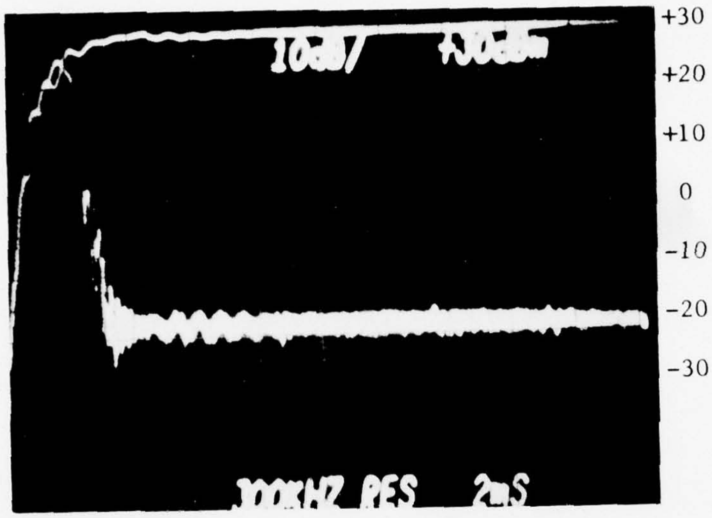


FIGURE 15

f = 21 MHz
MOD CW

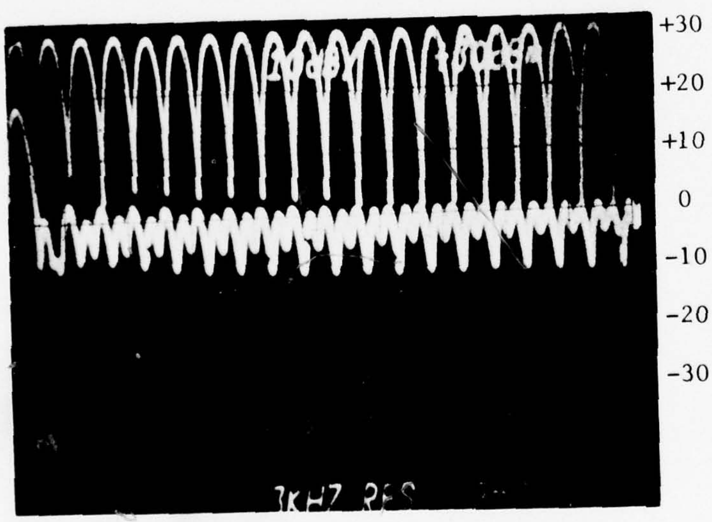


FIGURE 16

f = 3.6 MHz
MOD TWO-TONE
1 kHz SSB

ICS OUTPUT:
NULLING TIME TEST
(Para. 4.4.2)

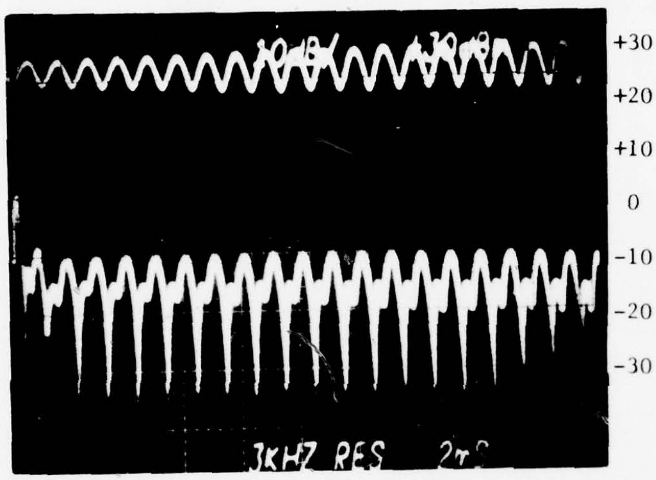


FIGURE 17

f = 14 MHz
MOD TWO-TONE
1 kHz SSB

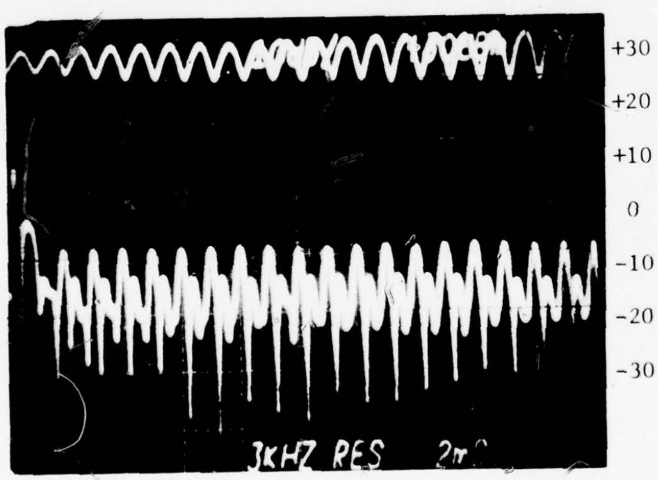


FIGURE 18

f = 21 MHz
MOD TWO-TONE
1 kHz SSB

Figure 19B shows the implementation using available equipment to subject the HFICS to signal levels of the same order as encountered in Figure 19A. Neither the 7 dB directional couplers or the +60 dBm transmitters are available for this test.

Record the degree of cancellation in each channel, with one and two transmitters operating.

Record the intermodulation (IM) products at the receive port with and without the HFICS operating.

4.5.2 Test Results

The photograph of Figure 20 shows two uncancelled signals at 7.0 and 7.2 MHz. The difference in amplitude is attributable to the difference in insertion loss of the vario couplers.

Figure 21 shows the residue after cancellation. Both fundamental signals are cancelled 50 dB. Unfortunately, the canceller gives rise to a series of harmonics. These harmonics could have been minimized by mechanically tunable filters within the weight, since they occur prior to cancellation. However, such filters were beyond the scope of an all-electronic canceller (see Section 5.2).

In the photograph of Figure 22 the spectrum analyzer sweep has been reduced to 200 kHz per division and the sensitivity has been increased 30 dB. A family of intermodulation products is apparent. These particular products were generated within the canceller. However, a similar family will also be generated within the transmitters unless the antennas are exceptionally well isolated.

These intermodulation products will normally preclude operating with two transmitters closely spaced in frequency. The amplitude and spacing of the intermodulation products make frequency management difficult.

Figures 23 and 24 show a similar test with the signals at 7.0 and 14.9 MHz, respectively. The signals were lower because of higher insertion loss of the vario couplers. Cancellation was only 28 dB at 7 MHz and 39 dB at 14.9 MHz. Note that the second harmonic of the 7 MHz interference appears at the ICS output at a power level which is 14 dB larger than the 7 MHz residue. The reason for the relatively poor performance compared to the two-tone test at 7 MHz is likely due to the presence of the 14 MHz harmonic in the ICS feedback error waveform.

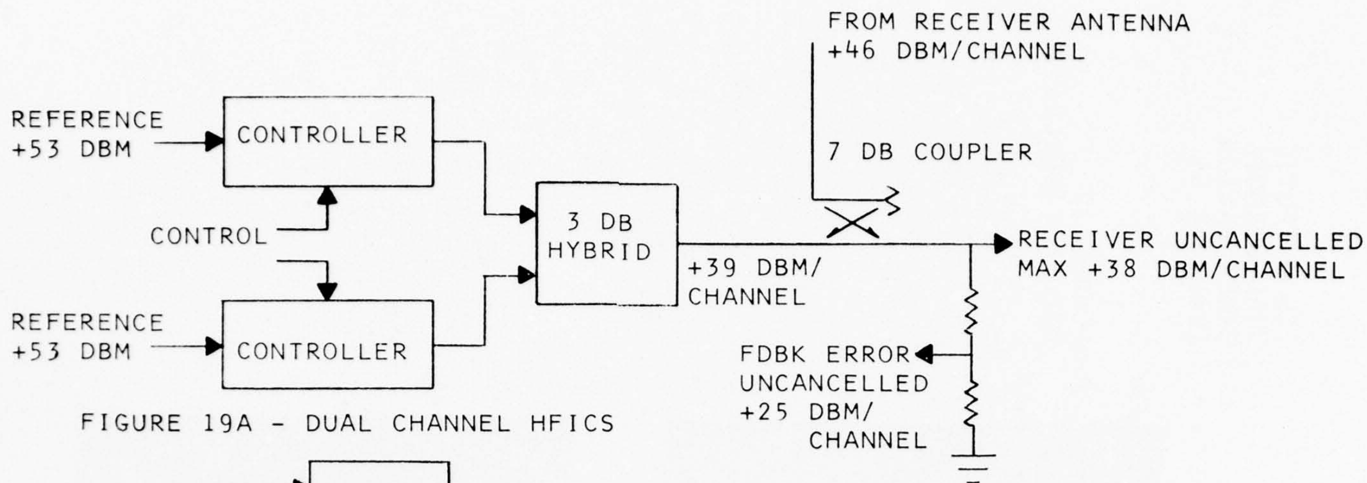


FIGURE 19A - DUAL CHANNEL HFICS

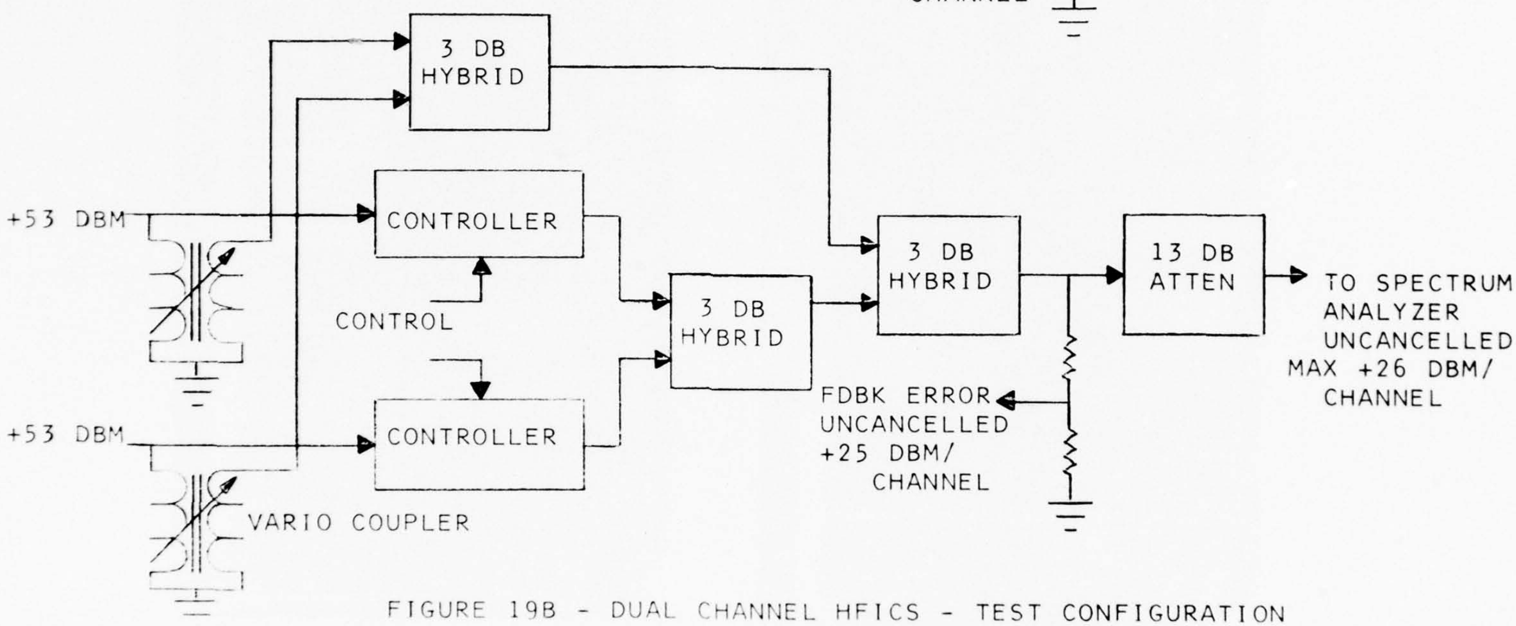


FIGURE 19B - DUAL CHANNEL HFICS - TEST CONFIGURATION

ICS OUTPUT:
DUAL CHANNEL
CANCELLATION
(Para. 4.5)

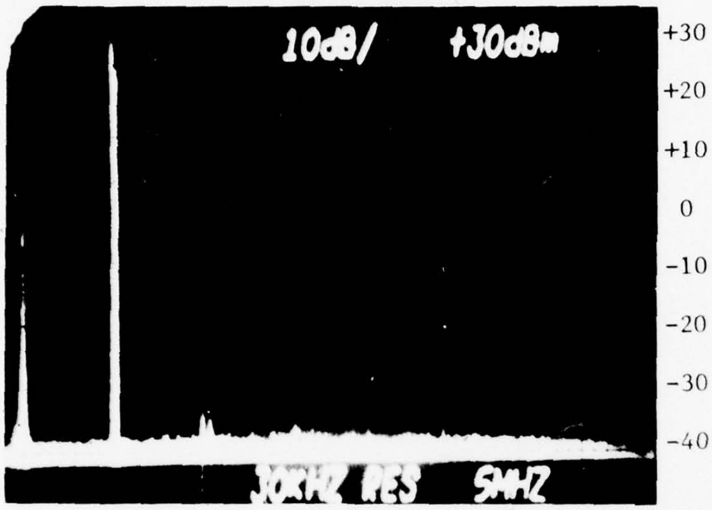


FIGURE 20
BEFORE CANCELLATION

f_1 = 7.0 MHz
f_2 = 7.2 MHz

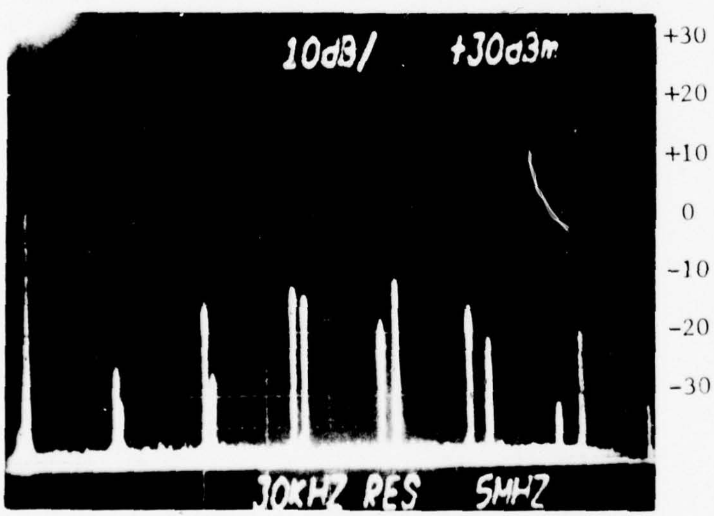


FIGURE 21
CANCELLED RESIDUE

f_1 = 7.0 MHz
f_2 = 7.2 MHz

ICS OUTPUT:
DUAL CHANNEL
CANCELLATION
(Para. 4.5)

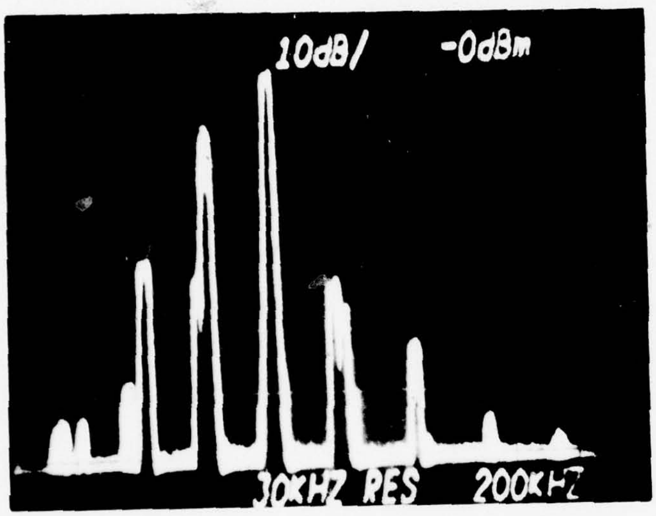


FIGURE 22
CANCELLED RESIDUE
INCREASED SENSITIVITY
INCREASED RESOLUTION

f_1 = 7.0 MHz
f_2 = 7.2 MHz

ICS OUTPUT:
DUAL CHANNEL
CANCELLATION
(Para. 4.5)

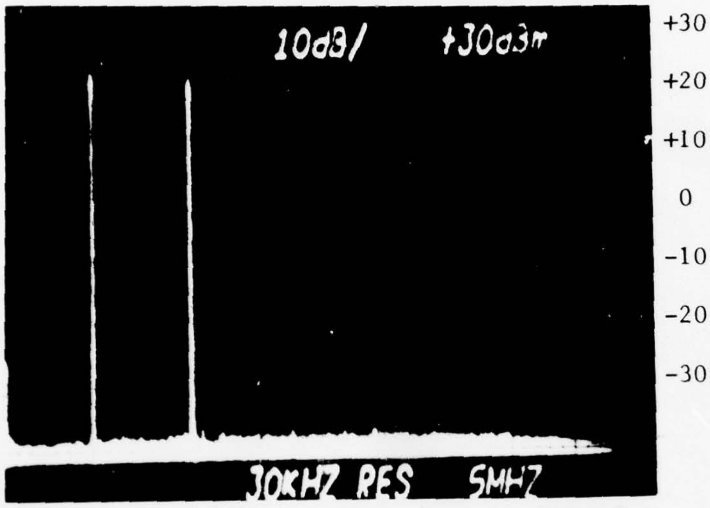


FIGURE 23
BEFORE CANCELLATION

f_1 = 7.0 MHz
f_2 = 14.9 MHz

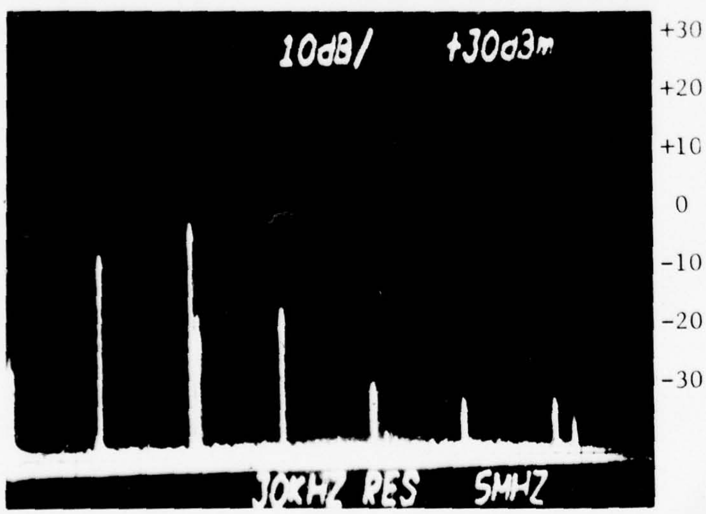


FIGURE 24
CANCELLED RESIDUE

f_1 = 7.0 MHz
f_2 = 14.9 MHz

4.6 INSERTION LOSS TO THE DESIRED SIGNAL

4.6.1 Design Goal

No greater than 8 dB exclusive of any amplifier.

This is a test of the 7 dB directional coupler which will not be available. The design parameters indicate that this requirement will be met if the coupler meets specification.

4.6.2 Test Results

The 7 dB directional coupler was not available at test time.

4.7 INTERFERENCE CANCELLATION TEST

4.7.1 Design Goal

Cancellation: 70 dB (CW); 55 dB (80% AM modulation).

A study of HF practice indicates that AM transmission is rarely used. For these tests a two-tone test is substituted. It should be noted in evaluating the results that a two-tone SSB test is a very severe test. It, too, is a condition rarely encountered in practice. However, it does represent a worst-case SSB evaluation.

In performing the two-tone test, the PEP is kept the same as that encountered with the CW test. Each tone is set 6 dB below that used for a single-tone test. The test is run with the test setup shown in Figure 12.

The two tests are run with 1 kHz spacing between the audio tones. Cancellation ratios are recorded for interferences at the following frequencies: 3.6, 7.0, 14 and 21 MHz (test equipment limitation).

4.7.2 Test Results

The data presented are photographs of the spectrum analyzer display of the ICS output. In Figures 25 through 32 the upper and lower traces represent the ICS output interference levels before and after cancellation, respectively.

Frequency	Cancellation Achieved	
	CW	Two-Tone
3.6 MHz	53 dB	28 dB
7.0	48	30
14.0	52	43
21.0	47	40
28.0	49	

CANCELLATION OF
INTERFERING SIGNAL
(Para. 4.7)

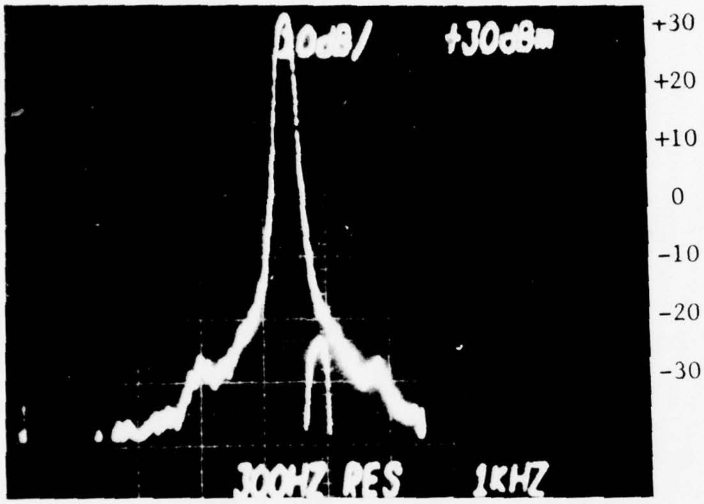


FIGURE 25

f = 3.6 MHz
MOD CW

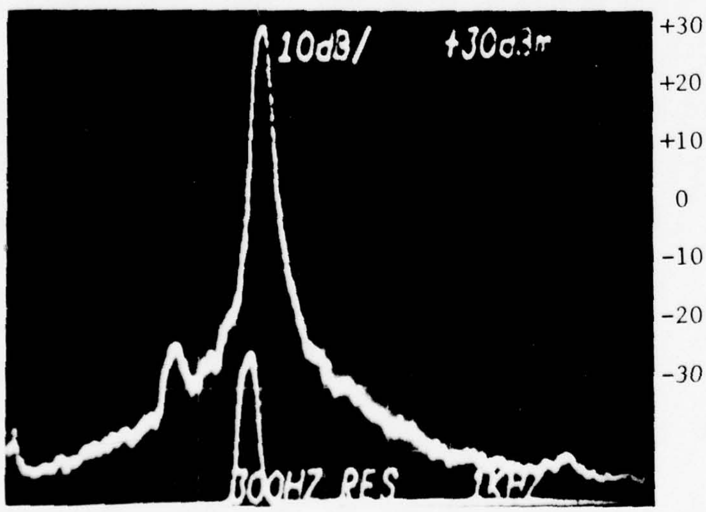


FIGURE 26

f = 7.0 MHz
MOD CW

CANCELLATION OF
INTERFERING SIGNAL
(Para. 4.7)

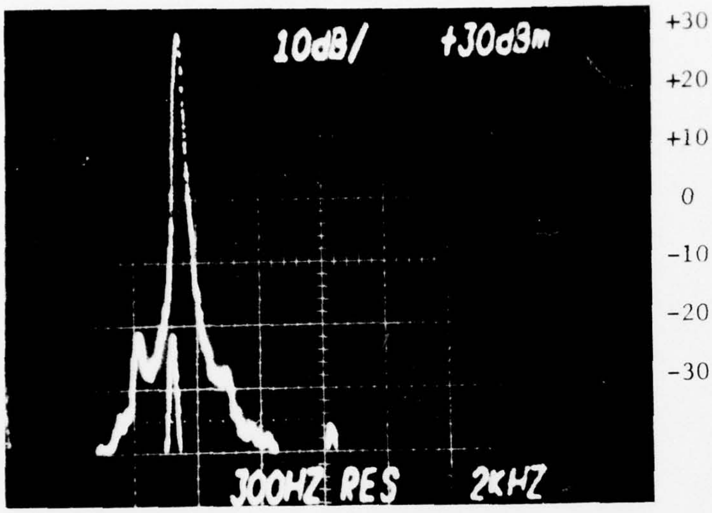


FIGURE 27

f = 14 MHz
MOD CW

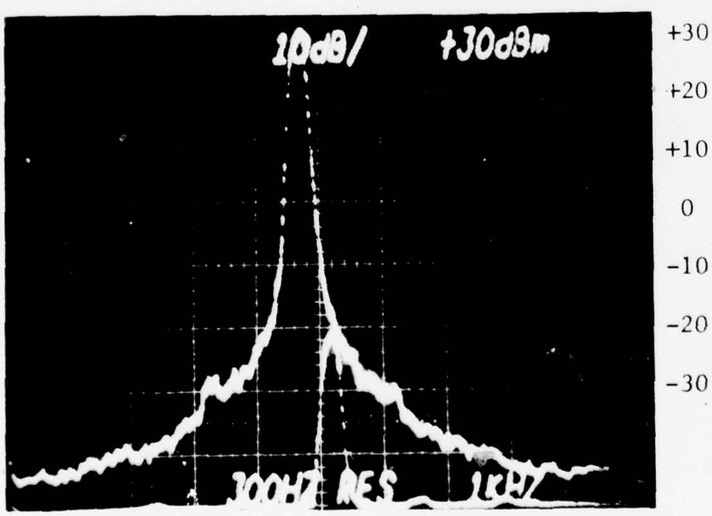


FIGURE 28

f = 21 MHz
MOD CW

CANCELLATION OF
INTERFERING SIGNALS
(Para. 4.7)

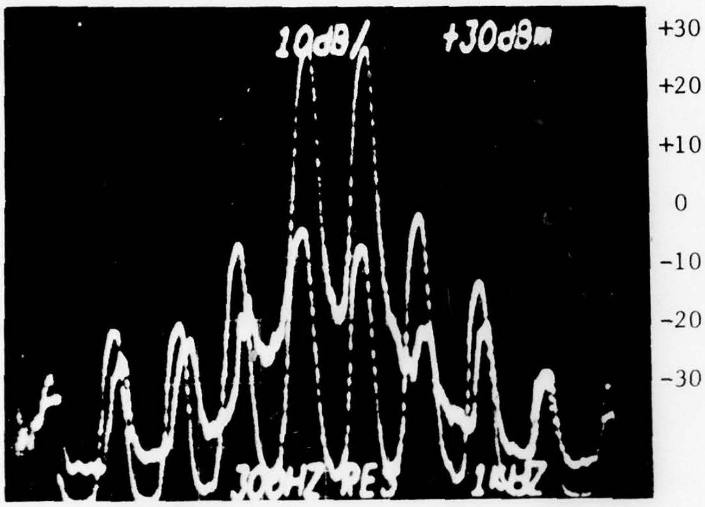


FIGURE 29

f = 3.6 MHz
MOD TWO-TONES
1 kHz SSB

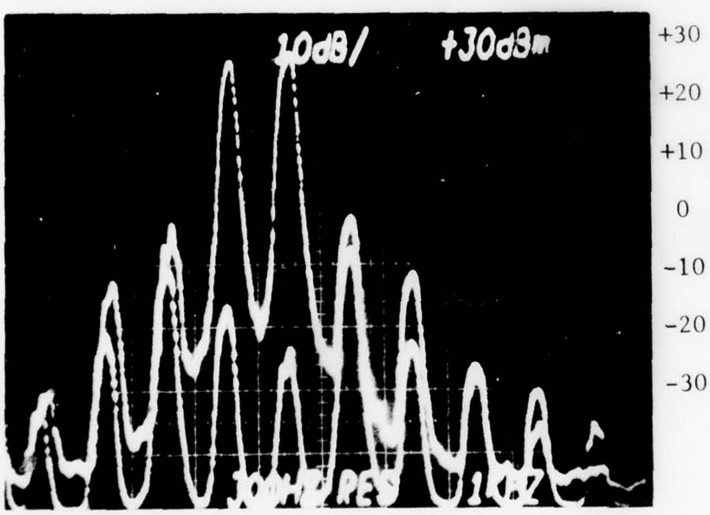


FIGURE 30

f = 7 MHz
MOD TWO-TONES
1 kHz SSB

CANCELLATION OF
INTERFERING SIGNALS
(Para. 4.7)

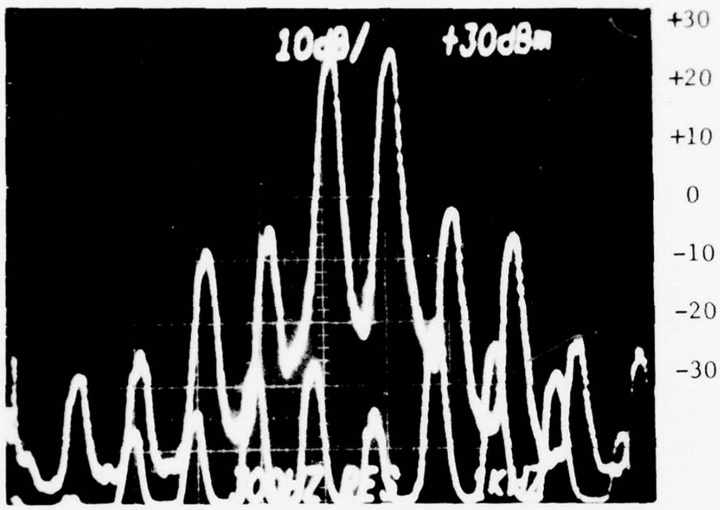


FIGURE 31

f = 14.0 MHz
MOD TWO-TONES
1 kHz SSB

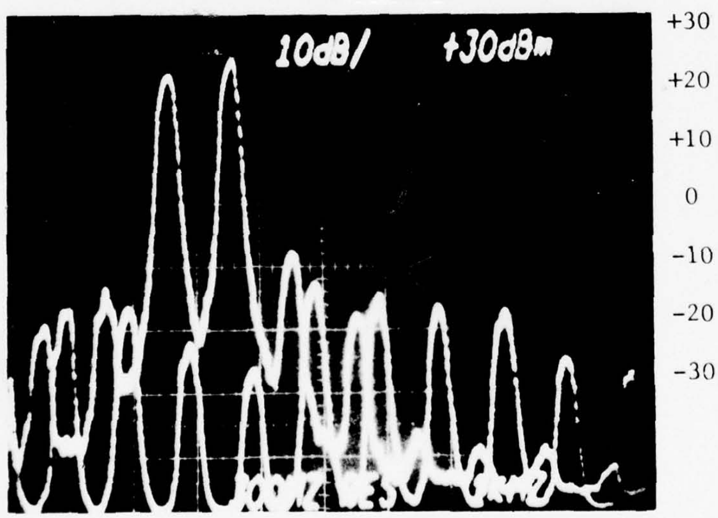


FIGURE 32

f = 21.0 MHz
MOD TWO-TONES
1 kHz SSB

In the two-tone test, cancellation is appreciably poorer at the low end of the band. The two-tone test is a worst-case bound for all modulation formats. FSK, pseudo RM and multitone SSB will all approach CW performance. In the latter case, the average power is much lower than that in the two-tone test.

The photographs of the two tests reveal the effect of ICS distortion on cancellation. Since this distortion occurs in the PIN diodes, the problem is greatest at the lower frequencies. At 3.6 MHz, Figure 30, the third-order intermodulation products introduced by the canceller exceed those coming from the transmitter prior to cancellation. By 7.0 MHz (see Figure 32), the ICS intermod products have dropped below those in the uncancelled signal. These intermodulation products limit HF cancellation performance.

4.8 WEIGHT OF THE TWO-CHANNEL HFICS

4.8.1 Design Goal

Less than 150 pounds.

The HFICS is placed on a scale.

4.8.2 Test Results

The two-channel HFICS weighs 115 pounds. While this is 35 pounds less than the design goal, it should be noted that no effort was made to minimize weight in this model.

4.9 MEASUREMENT OF NOISE AND SPURIOUS GENERATED BY THE ICS AT ITS OUTPUT

4.9.1 Design Goal

Less than -115 d Bm in a 12 kHz band 100 kHz or greater removed from a colocated transmitter.

The HFICS is designed to minimize the generation of noise and internally generated spurious. It contains no RF amplifiers and no chopper circuits. To the extent that the high power controllers are nonlinear devices, they will generate harmonics and intermodulation products when multiple tones are present.

This section covers the measurement of the noise and spurious signals generated by the HFICS. The spurious products are power level sensitive. The worst case is examined in this section.

In the measurement of both noise and spurious it is necessary to distinguish between those signals originating in the test generators and those originating in the HFICS. The noise measurement presents a particularly difficult problem.

When the HFICS is structured for use with a +60 dBm transmitter with 14 dB of space loss between the transmitting and receiving antennas, the uncancelled residue at the receive port is +39 dBm. If 50 dB of cancellation is assumed, the cancelled residue is -11 dBm or 104 dB above the design goal.

The Tektronix 7L12 spectrum analyzer is limited to 80 dB dynamic range and measurement at either 3 kHz or 30 kHz IF bandwidth. The noise figure is about 16 dB which also presents a problem. At maximum sensitivity the bottom line is -110 dBm.

To minimize the latter problems, an ENI 500P preamplifier is used. This amplifier has a nominal gain of 27 dB and a noise figure of 8 dB. The noise from the preamplifier is -125 dBm/12 kHz. The HFICS is assumed to be in specification if the residual noise is not more than 10 dB greater than the amplifier noise. The test is run at 3 kHz bandwidth for resolution. This leaves the dynamic range of the analyzer and the residual noise from the test transmitter.

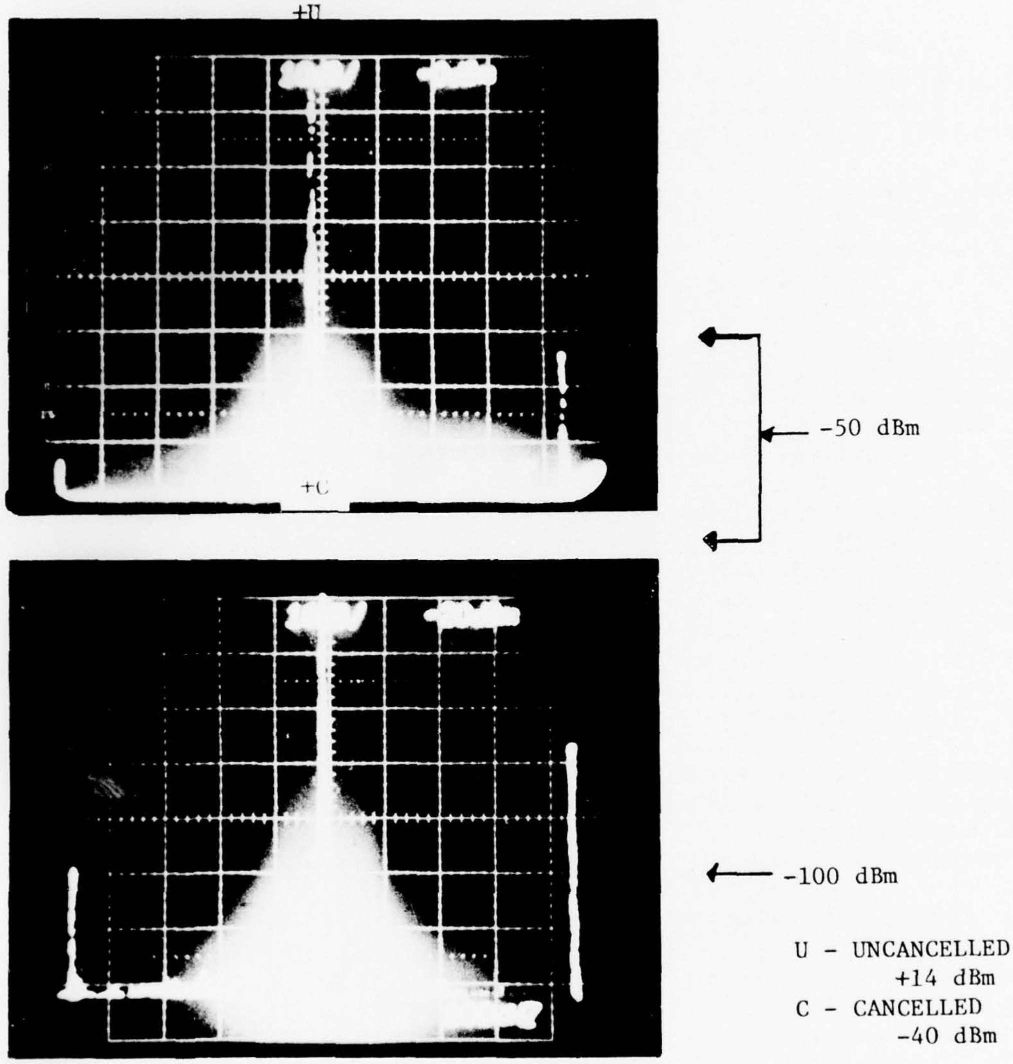
Since the uncancelled noise from the transmitter is well above the design goal, measurement depends on cancellation of the transmitter noise. The transmitter noise level decreases with frequency offset, but so does the cancellation.

In order to evaluate the noise level, the system was set up as a single-loop canceller for simultaneous transmission and reception on a common antenna. The transmitter power is reduced to 200 watts to simulate the Collins 618T2 transmitter used on many military aircraft. Under these conditions it is possible to remain within the dynamic range of the measurement equipment. However, there is no way to distinguish between the cancelled noise from the test transmitter and that contributed by the HFICS.

The noise test setup is shown in Figure 33. The test setup in Figure 12 is used for the remainder of the tests for spurious signals.

4.9.2 Test Results

Figure 33 shows that the HFICS is capable of cancelling the noise from a KWM2A transmitter below the design goal level under the test conditions. It follows that the noise contribution of the HFICS is within specification since the photograph shows the sum of the transmitter and HFICS noise contributions after cancellation.



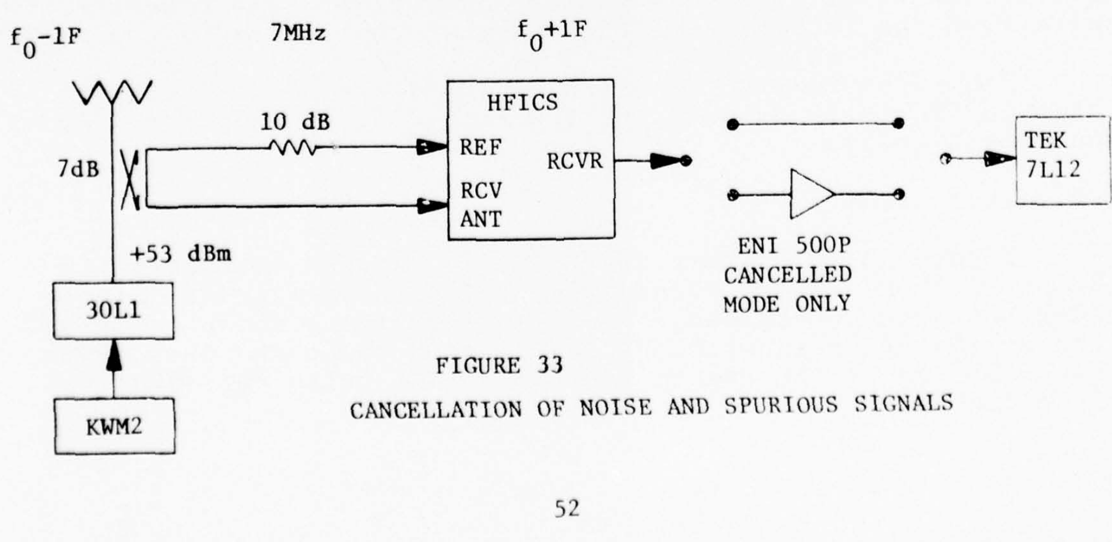


FIGURE 33

CANCELLATION OF NOISE AND SPURIOUS SIGNALS

The spurious ±455 kHz removed from the transmit signal require consideration. These originate in the transmitter. Their presence brings out the necessity for frequency management in avoiding transmitting spurious as well as receive spurious response when assigning frequencies for full-duplex operation with the HFICS.

At full power level the generation of harmonics and intermodulation products are limiting factors in the employment of the HFICS.

Figure 22 shows intermod residue in a dual channel system. Figures 29 through 32 show that the third-order intermodulation products in the cancelled residue in a two-tone SSB test are quite large. In the two-channel system, frequency management appears to be the only solution, i.e., avoiding reception at a third-order intermodulation product.

A two-tone SSB test is unusually severe. With the usual SSB signal, the intermod residue will be much lower. With CW, FSK, or quasi FM the problem does not exist. With SSB the intermod residue may limit the minimum transmit-receiver spacing.

The harmonics generated by the HFICS exceed those expected from the transmitter. They generally exceed the cancelled fundamental. The harmonics generated by the transmitted are normally of sufficient magnitude to preclude receiving at a transmitter harmonic. The HFICS contributes to this problem.

The condition is most serious at the low end of the band. Figure 34 shows the harmonic level in the uncancelled signal at 3.6 MHz. Figure 35 shows the increase in the harmonic level after cancellation. The photo of Figure 36 shows the drop in the harmonic level for a 10 dB drop in reference power and interference level. Note that the fundamental is not cancelled as well, indicating insufficient loop gain at this lower operating level.

Figures 37 through 40 cover the residue for 7 and 14 MHz fundamental signals. The harmonics of higher frequency HF signals fall out of the HF band.

In all cases, the third harmonic is the highest level residue. Its amplitude decreases with increasing frequency. The third harmonic residue level for a transmitter at 3.6 MHz is 18 dB higher than for one at 14 MHz. In all cases, the harmonics introduced by the HFICS are larger than those introduced by the transmitter. This is understandable since the transmitter output is filtered. A similar treatment for the HFICS should result in a similar reduction of harmonic components in the cancelled residue.

SPURIOUS SIGNALS
(Para. 4.9)

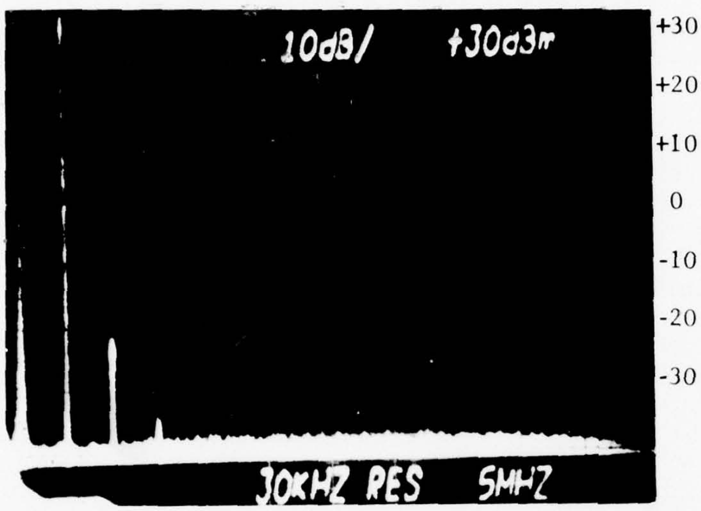


FIGURE 34
UNCANCELLED SIGNAL

f = 3.6 MHz
200 WATT REFERENCE

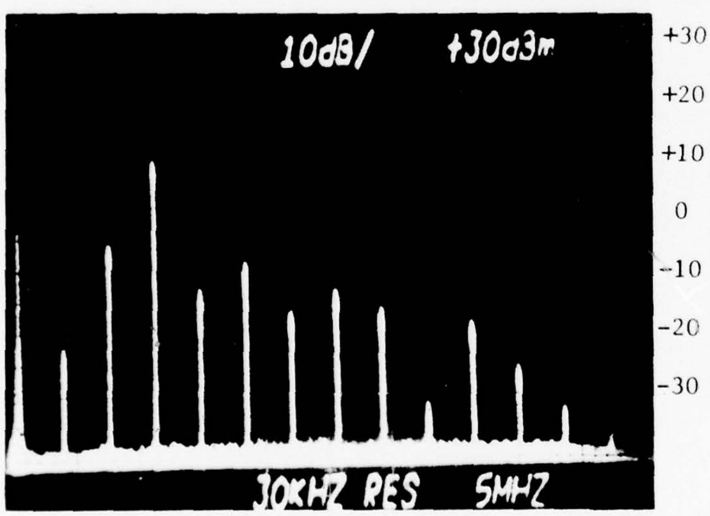
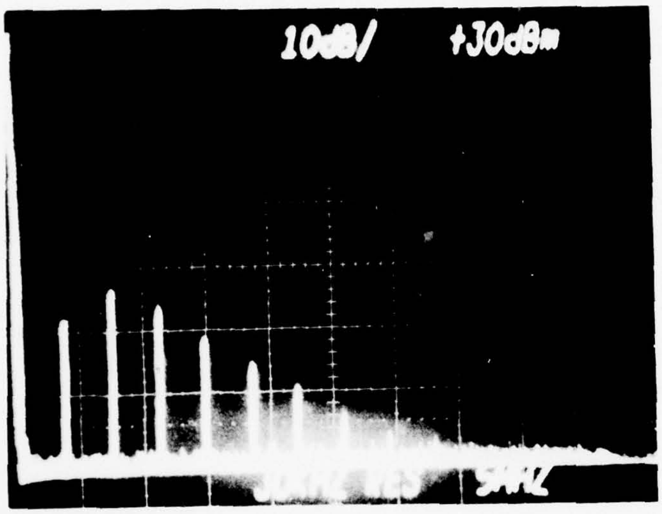


FIGURE 35
CANCELLED RESIDUE

f = 3.6 MHz
200 WATT REFERENCE

SPURIOUS SIGNALS
(Para. 4.9)



+30
+20
+10
0
-10
-20
-30

FIGURE 36
CANCELLED RESIDUE AFTER
10 dB REDUCTION IN POWER
LEVEL BELOW FIGURE 35

20 WATT REFERENCE

SPURIOUS SIGNALS
(Para. 4.9)

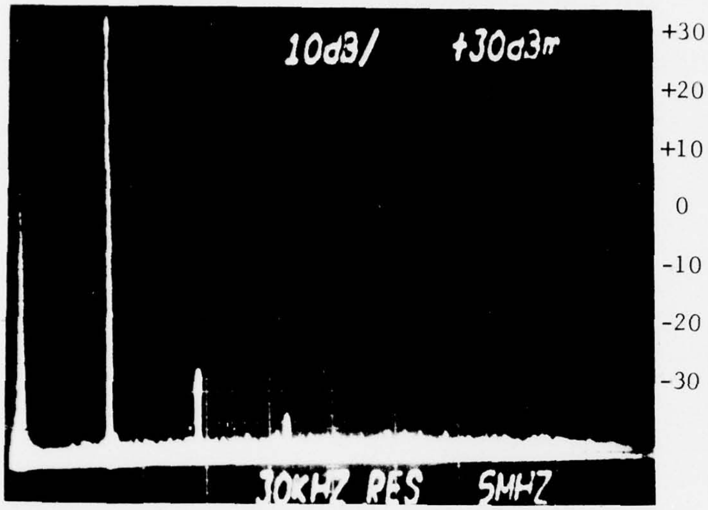


FIGURE 37
UNCANCELLED SIGNAL

f = 7 MHz

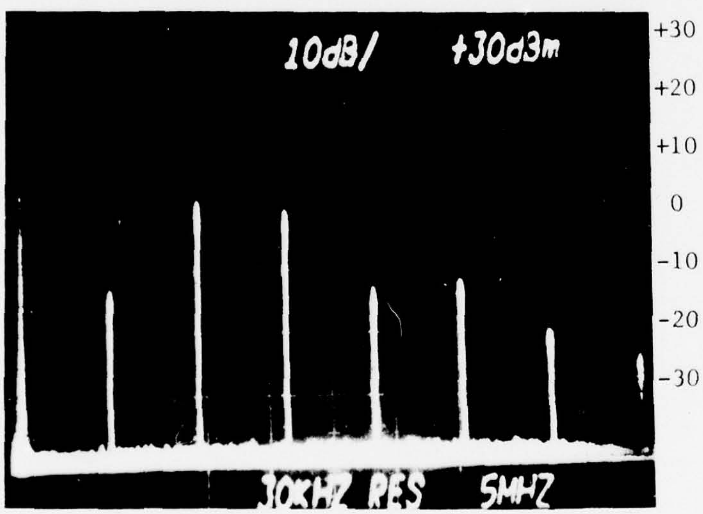


FIGURE 38
CANCELLED RESIDUE

f = 7 MHz

SPURIOUS SIGNALS
(Para. 4.9)

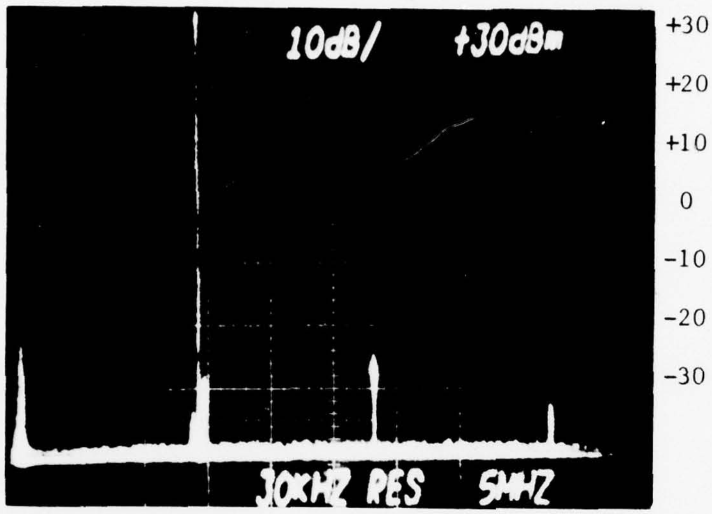


FIGURE 39
UNCANCELLED SIGNAL

f = 14 MHz

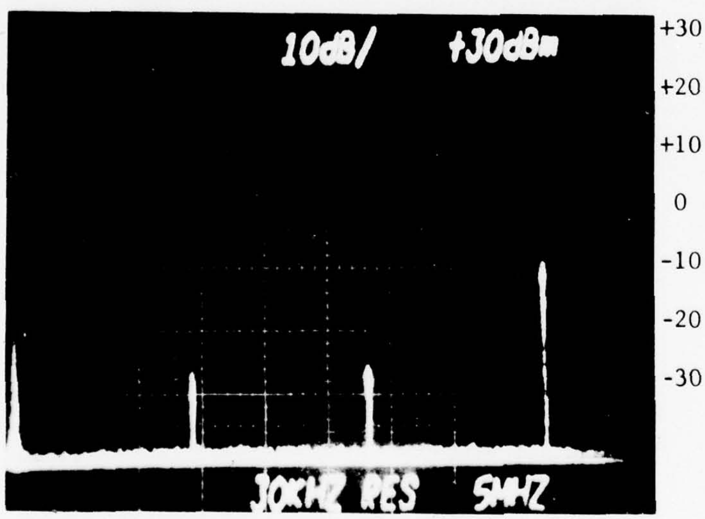


FIGURE 40
CANCELLED RESIDUE

f = 14 MHz

4.10 SERVO CONTROL POWER MEASUREMENT

4.10.1 Design Goal

No greater than 200 watts/ICS.

Measure the maximum power consumption of the Dual Channel HFICS by connecting a wattmeter in the power source.

4.10.2 Test Results

The prime power consumption measures 4.5 amperes at 115 volts or 517 watts for the dual-channel HFICS or 29 percent over the design goal. The power supply was over-specified in this model in order to use an off-the-shelf supply.

SECTION 5 - HFICS OPERATIONAL CONSIDERATIONS

Described below are factors which affect the design and performance of an HFICS.

5.1 HF TRANSMITTER

Narrowband filtering is desirable at the transmitter output to minimize the level of transmitter noise and harmonics radiated. Intermodulation products generated at the transmitter as a result of coupling between transmitter antennas will not be suppressed.

Interference cancellation improves with increasing frequency. Operation at the low end of the HF band may require additional filtering of interference harmonics in the controller for optimum performance.

Cancellation is best with a constant envelope interference.

Dual transmitter operation, in addition to the introduction of a family of intermod products, will also degrade the cancellation performance for each fundamental interference. Additional filtering will improve cancellation, but will not suppress intermodulation products introduced externally to the HFICS.

5.2 HFICS

Cancellation performance may be improved by reducing the level of the interfering signal prior to cancellation. The level of the interfering signal can be attenuated without appreciably degrading receiver performance for those cases in which the ambient noise level exceeds the receiver noise floor. Since both the ICS and the receiver are nonlinear devices, attenuation ahead of the ICS can result in improved receiver sensitivity in the face of an interfering transmitter even though the attenuation is sufficient to degrade reception when there is no interference (see para. 5.5).

Cancellation performance may be improved by filtering the ICS controllers to minimize harmonic products and, in the case of dual channel operation, HFICS-generated intermodulation products.

The high power controllers are the sources of intermodulation and harmonic distortion in the ICS. These devices are designated by W in Figure 4.

In a dual channel HFICS, there is cross-coupling between the controllers through the imperfect isolation afforded by the quadrature hybrid QH. This coupling results in third-order intermodulation products as shown in Figure 22. It should be noted that such products will also be formed in the transmitters as a result of coupling between the transmitting antennas. Provided the frequency separation between the interfering transmitters is sufficient, the high power controllers can be isolated and the harmonics attenuated by means of filters following the high power controller. Either lowpass or bandpass filters may be used. Lowpass filters introduce insertion phase shift as a function of frequency. A lowpass filter following the controller requires a compensating filter in the correlator leg. A bandpass filter does not necessarily introduce insertion phase at band center. It can be introduced after the controller without affecting the cancellation for a CW signal.

For wideband signals, the effect of the bandpass filter on the cancellation notch bandwidth must be considered. With the cancellation notch at the center of the bandpass filter, the cancellation residue is largely accounted for by the phase error introduced by the filter. For a filter

$$t_g \triangleq \frac{d\phi}{d\omega}$$

Typical values of t_g for a normalized (equivalent lowpass BW = 1 rad/sec) Butterworth filter are one second for a one-pole filter and two for a three-pole filter.

For a bandpass filter ω is normalized to $\omega/(\omega_c-\omega_0)$. After integrating from ω_c to ω_0

$$\phi = t_g \frac{\omega-\omega_0}{\omega_c-\omega_0}$$

But

$$Q \triangleq \frac{\omega_0}{2(\omega_c-\omega_0)}$$

Then

$$\phi = t_g \frac{2(\omega-\omega_0)}{\omega_0} Q$$

Let ω_0 be the center of the cancellation notch and ω be one edge of the bandwidth over which the cancellation notch is to be measured. Then the normalized cancellation notch bandwidth B is $2(\omega-\omega_0)/\omega_0$.

$$\phi = t_g \; Q \; B$$

For small values of ϕ the cancellation ratio is limited to $CR = 20 \log \phi$ by the phase error. At the band edges

$$CR = 20 \log t_g Q B$$

It can be shown that the integrated value of the cancellation ratio is 5 dB lower for an equal power level interference within the notch

$$CR = (20 \log t_g QB-5) \text{ dB}$$

Consider a three-pole Butterworth filter with a Q of 2 and a 3 MHz interference 3 kHz wide ($B=10^{-3}$). The cancellation ratio will be limited to -53 dB by the filter. Such a filter will reduce the second harmonic residue by 36 dB and the third harmonic by 54 dB. This is more than adequate to reduce the harmonic residue well below the fundamental cancellation residue (see Figures 21 and 35).

In the dual canceller mode, such filters will reduce the third-order distortion products between transmitter signals provided the two interfering signals are spaced sufficiently to permit the filters to provide adequate isolation. Since these filters would be introduced after the high power controllers, the maximum power through each filter would be 30 watts.

The required tuning accuracy is not great. Small amounts of mistuning will be evidenced by a reduction in cancellation loop gain due to the insertion phase of the filter. The reduction in loop gain is equal to 20 log cos ϕ, where ϕ is the insertion phase of the filter in radians. For example, a phase error of 0.5 radian only reduces the loop gain about 1 dB.

The power level precluded implementing such filters without resorting to electromechanical tuning. Electromechanical tuning is beyond the scope of this effort.

Reducing the design power level drops the higher harmonic levels at an even greater rate. Figures 35 and 36 show a reduction in third harmonic level of about 25 dB for a 10 dB reduction in reference power. Conclusions regarding the second harmonic are misleading, since the second harmonic residue is a function of balance within the high power controller. The Q of the required filter as well as the necessity for filters is dependent on the design interference level.

5.3 ANTENNAS AND ATMOSPHERIC NOISE

Space loss between transmit and receive antennas should be determined as a function of transmit frequency to permit system optimization.

The expected ambient noise level over the operating frequency range should be determined. Attenuation of desired signal,

interfering signal, and ambient noise down to the receiver noise floor will have minimal effect on receiver performance. It will have a major effect on both cancellation implementation and performance.

For discussion purposes the following noise level table for a quiet location will be used (conservative).

2 MHz	-100 dBm/3 kHz
4 MHz	-102 dBm/3 kHz
8 MHz	-106 dBm/3 kHz
20 MHz	-125 dBm/3 kHz
30 MHz	-133 dBm/3 kHz

Typical receiver noise floor is -126 dBm/3 kHz.

5.4 LONG RANGE SIMULTANEOUS TRANSMISSION AND RECEPTION

For long range communication, the region between the maximum usable frequency (MUF) and the lowest useful frequency (LUF) is normally restricted to a relatively narrow band of frequencies.* The usable window will often be as narrow as 2 MHz. Receive-transmit isolation by filter techniques becomes impractical when the transmit-receive offset falls below 10% of the transmit frequency.

The HFICS may be considered as a selective notch filter which selectively notches out the interfering signal including some of its close-in noise contribution without degrading the receive signal-to-noise ratio. For optimum operation, the transmitter signal should be bandlimited to minimize transmit noise contribution outside of the HFICS cancellation notch.

5.5 HF RECEIVERS, TRANSMITTERS, AND AMBIENT NOISE

At this point, a discussion of typical HF transmitter and receiver characteristics is in order. A 1 kW vacuum tube transmitter will normally consist of an exciter, driver, and linear power amplifier with an overall gain of about 60 dB. The close-in noise level will be about -142 dBc/Hz or -47 dBm/3 kHz (see para. 4.9.1).

Bandlimiting will vary with transmitters. Typically, the filter will consist of a double-tuned interstage between the driver and the power amplifier and a double-tuned coupling network between the power amplifier and the transmission line to the antenna coupler. The bandwidth will vary from about 1/2 MHz at

*ESSA Technical Report IER 1-ITSA1 (AD644827).

2 MHz to about 3 MHz at 30 MHz. Solid state transmitters are not so filtered. The noise level is essentially independent of frequency offset and comparable to the close-in noise level of a vacuum tube transmitter.

HF receivers fall into two general categories: all-electronic and electromechanical. The latter provide appreciable RF filtering; RF protection in the former is limited to switched filters, usually one-half octave wide.

The Collins 635V-1 receiver tuner is representative of what can be done with a good electromechanical design. Such a filter will permit HF reception with a 1000-volt interference removed 10% in frequency. It is of little help when the interference falls within its passband.

Because of the high ambient noise level, there is little reason for exceptional receiver noise figures. A typical noise figure is 13 dB, resulting in a threshold SSB sensitivity of -116 dBm (10 dB signal-to-noise ratio at a 2.7 kHz BW).

The remaining all-electronic RF implementation is usually an AGC-controlled attenuator, an upconverter followed by a crystal filter ahead of the first IF. Typically, the first IF bandwidth is 16 kHz with an ultimate rejection of 80 dB.

Outside of the IF filter, the receiver's immunity to high level interference does not change markedly until the added protection of the switched preselector filter is reached. For discussion purposes, it will be assumed that the threshold sensitivity will start to degrade when an interference 80 dB above threshold falls into this unprotected band. Expected performance can be scaled to the performance of the receiver designated for the system. For example, the RACAL 6217A spurious response is specified as better than 60 dB down for signals less than 10% off tune and 80 dB for signals more than 10% off tune. The newer Collins HF8050/8050A spurious response specification is -80 dB min. at 20 kHz or more off center frequency.

It is well-known that the HF environment is noisy. For shipboard systems a quasi-minimum noise level has been established.* The word "minimum" is used advisedly; conditions are usually worse. The Quasi-Minimum Noise Level in dBm/kHz is -92 at 2 MHz and -124 at 30 MHz. The level fits the equation

$$Q\text{-}M = -[27 \log f_{MHz} + 84] \text{ dBm/kHz}$$

*NELC Technical Note TN 2435, "Shipboard Noise Measurements," 18 July 1973.

Similar data are not readily available for aircraft installations. In any event, aircraft reception will be limited by atmospheric noise. Atmospheric noise levels are highly variable (CCIR Report 322, 10th Plenary Assembly, Geneva, 1963, covers the expected range). Section 5.3 of this report presents noise levels to be expected in a quiet location during daytime. The noise increases markedly at night.

For discussion purposes, the problem of communication in a window around 3 MHz will be covered. The assumptions are that the transmit-receive antenna isolation is 14 dB, and thus isolation is invariant with frequency. The transmitter harmonics start off 40 dB down and fall off at 12 dB per octave. The atmospheric noise level is that shown in para. 5.3.

A 13 dB pad is placed in the receive antenna path to increase the total attenuation between the transmit antenna and the receiver to 35 dB. Removal of the 13 dB pad will not improve the sensitivity referred to the antenna, since the sensitivity is limited by the uncancelled residue. Interference levels at the receiver input at 3 MHz are:

Uncancelled XMIT signal	+25 dBm
XMIT noise level (uncancelled)	-82 dBm/3 kHz
Ambient noise level	-122 dBm/3 kHz
Receiver noise floor	-126 dBm/3 kHz
Second harmonic	-15 dBm
Cancelled XMIT signal	-35 dBm*

The results of this analysis are shown in Figure 41. It will be noted that the uncancelled harmonics exceed the cancelled transmitter fundamental. Most HF receivers are equipped with half-octave RF filters. The harmonics should not cause problems for reception below about 4.5 MHz. The signal threshold shown is that for a 10 dB signal-to-noise ratio for the weakest component of the desired signal.

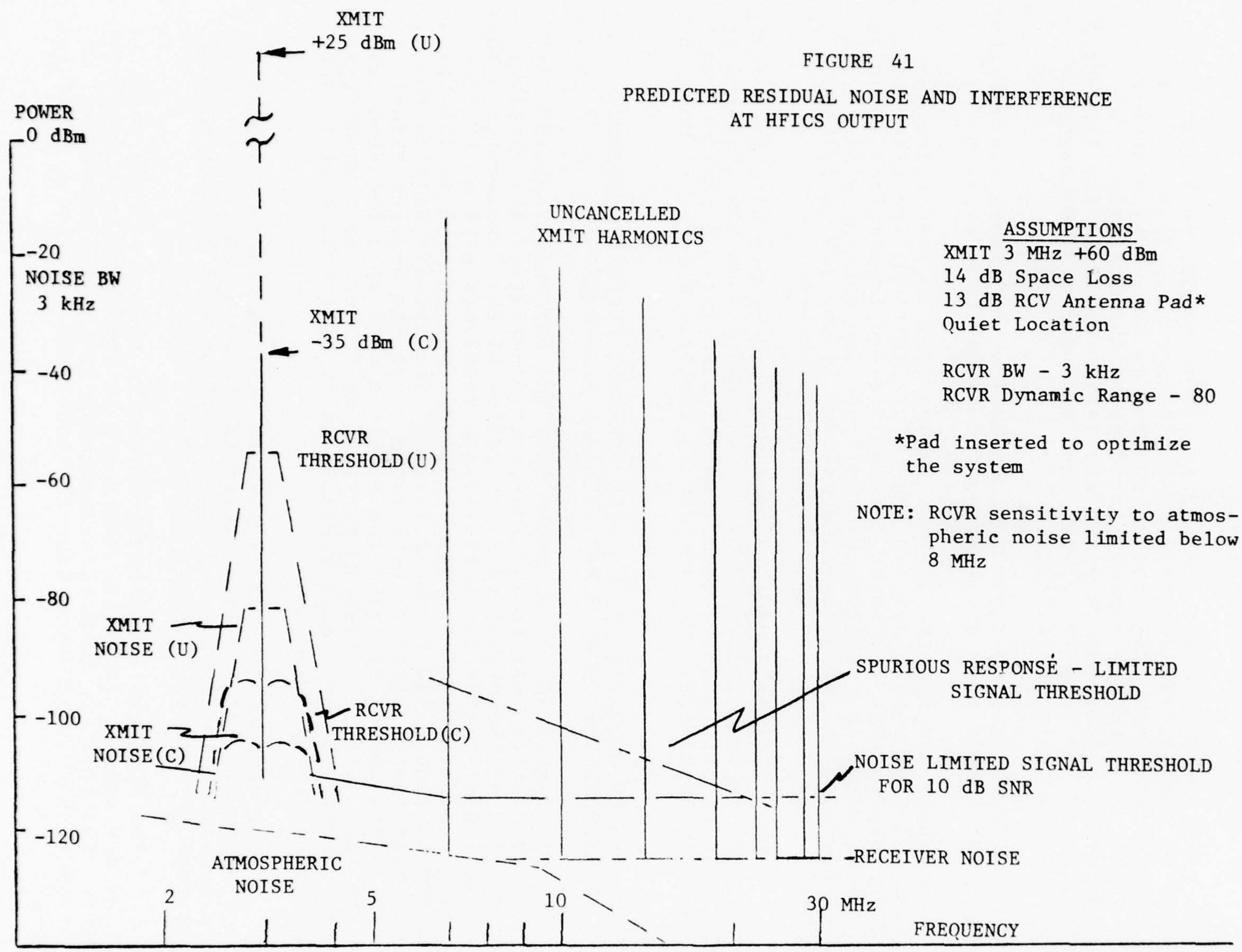
Transmitter broadband noise cancellation is estimated at 40 dB close-in which reduces the noise after cancellation to about the atmospheric noise level.

Figure 41 shows the predicted spectrum at the receiver input under the assumed conditions. Only the uncancelled transmitter noise is shown. Although close to the interfering signal, the ICS will reduce the noise residue and the signal threshold

*HFICS optimized to obtain 60 dB cancellation by reducing signal level and by adding filtering within the HFICS to eliminate HFICS-generated harmonics. This may be a much smaller HFICS. The RF power has been reduced to 5% of the original design goal by the 13 dB pad.

FIGURE 41

PREDICTED RESIDUAL NOISE AND INTERFERENCE
AT HFICS OUTPUT



ASSUMPTIONS
XMIT 3 MHz +60 dBm
14 dB Space Loss
13 dB RCV Antenna Pad*
Quiet Location

RCVR BW - 3 kHz
RCVR Dynamic Range - 80

*Pad inserted to optimize the system

NOTE: RCVR sensitivity to atmospheric noise limited below 8 MHz

(U) UNCANCELLED (C) CANCELLED

will be improved correspondingly.

Note that the interfering signal is cancelled below the level of the interfering transmitter harmonics. This fact is of importance where the receive antenna is shared by a number of receivers tuned to various portions of the spectrum. The assumed 80 dB spurious response limitation will set the threshold sensitivity for those receivers when the uncancelled harmonics fall within their RF passband.

Figure 41 also shows that ambient noise limits the receiver threshold rather than attenuation for frequencies below 8 MHz.

There are several factors to consider in predicting the effect of attenuation above 8 MHz. For those XMIT-Receive frequency separations for which the uncancelled transmitter noise is the limitation in receiver threshold, no improvement will result by a decrease in input attenuation even if the ICS could cope equally well with the higher level interference.

The ICS-introduced distortion does decrease with increasing frequency so that less attenuation is required at the high end of the band to maintain the same level of cancellation residue and ICS-added harmonics. The subject is explored further in para. 5.6.

5.6 HFICS OPERATION WITH LARGE TRANSMIT-RECEIVE FREQUENCY SEPARATION OR WITH SURVEILLANCE RECEIVERS

In Figure 41 it was shown that the harmonic radiation from an HF transmitter may be sufficient to desensitize the receiver regardless of the degree of cancellation of the fundamental. This is particularly true for surveillance receivers with no RF filtering. Additional filtering should be incorporated in the transmitter to reduce the harmonic level at the receive antenna to less than the receiver dynamic range above the desired signal level. The amount of filtering required will be a function of space loss. If it proves impractical to filter the transmitter sufficiently, a more complex HFICS can be built which will cancel discrete harmonics.

For this section it is assumed that the harmonics have been attenuated at the transmitter to the point where they are not a desensitization factor and that reception will be limited to the regions between transmit harmonics.

The HFICS will introduce harmonics unless certain precautions are taken. These harmonics are introduced by the controllers. The level of harmonics generated in the ICS controller decreases both with increasing frequency and decreasing reference power.

It was shown in Section 5.4 that attenuation can be added in the receive signal path at the low end of the band without degrading receiver performance. A single-pole highpass filter with a cutoff at 12 MHz placed in both the reference and signal path will reduce both of these signals 16 dB at 2 MHz. Above 12 MHz, conditions will be little changed.

Based on the assumed ambient noise conditions and the 8 dB HFICS insertion loss, the highpass filter will not degrade receiver performance. It will reduce the uncancelled residue at 2 MHz, under the assumed conditions, from +38 dBm to +22 dBm. At higher frequencies, the uncancelled residue will increase. Assuming the space loss remains constant, the uncancelled residue will return to +38 dBm, above 12 MHz. In most installations, constant space loss is not a valid assumption. The likelihood is that the space loss will increase with frequency. Should this prove to be the case, the reference signal extracted from the transmitter can be decreased correspondingly from its present 200-watt level.

Figure 42 shows the measured level of the cancelled residue and internally generated harmonics present at the receiver port of an HFICS with a 12 MHz cutoff highpass filter in both the receive antenna and the reference line. No effort was made to compensate for the change in loop gain over the band for this test. (The data were previously report in R&D Status Report #13, dated 1 April 1976, on this contract.)

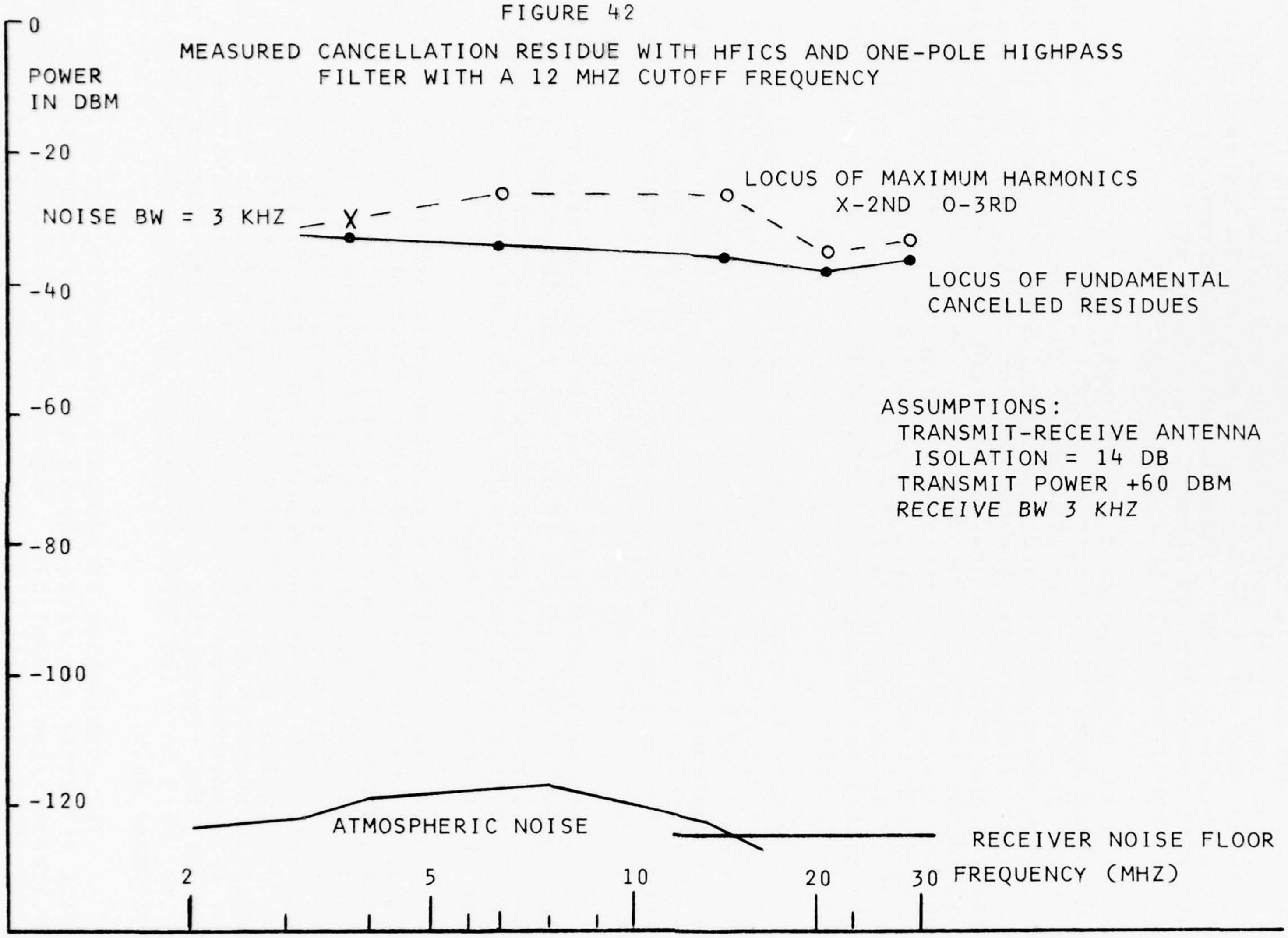
The atmospheric noise level exceeds the receiver noise floor below 12 MHz. Above 12 MHz the 8 dB insertion loss of the ICS will limit receiver performance in the absence of transmission. If this is a factor, a TR switch could bypass the HFICS when the transmitter is off.

For the surveillance receiver application, the harmonics introduced by the HFICS could limit sensitivity. Normally, the dynamic range of such a receiver will not exceed 80 dB. An HF transmitter at 12 MHz would limit sensitivity to -105 dBm (worst-case). If the transmitter is filtered so that its harmonics are well below -25 dBm at the receiver pot, the HFICS can be modified to include a set of half-octave filters similar to those normally supplied with HF receivers. These filters would follow the ICS controllers. They would be automatically switched to straddle the transmitter fundamental. Similar filters would also be switched into the HFICS correlator reference path to compensate for phase delay.

The combination of adequate transmitter filtering and the HFICS filtering described should make surveillance reception and HF transmission compatible. Without HFICS filtering, the level of the harmonics will limit maximum HF receiver performance to frequencies protected by the HF receiver half-octave filters.

FIGURE 42

MEASURED CANCELLATION RESIDUE WITH HFICS AND ONE-POLE HIGHPASS FILTER WITH A 12 MHZ CUTOFF FREQUENCY



The approach described in this section is also applicable to the problem covered in para. 5.4. The highpass filter replaces the attenuator introduced in that section.

5.7 DUAL-CHANNEL HFICS

Simultaneous cancellation of two HF transmitters introduces another dimension to the frequency management problem. In addition to the difficulty of reception at the harmonics of each transmitter, reception must also be avoided at the intermodulation products of the two transmitter frequencies.

With closely spaced transmit frequencies, the solution to the problem becomes more complex. It is well-known that intermodulation products will be generated within the transmitters when the antennas are in close proximity as on an aircraft. Narrowband filters at each transmitter, together with frequency spacing, will alleviate this problem.

The dual-channel HFICS, as implemented, will also introduce intermodulation products. The intermod levels are a function of the isolation of the combining hybrid. In practice, the lower order products are about the level of the cancelled fundamental residue. The approach suggested is similar to that outlined in para. 5.6. Since the problem is greatest at low frequencies, one can insert highpass filters in the receive and reference lines. These filters should be chosen to minimize receiver degradation just as in Section 5.6. The transmitter outputs should be filtered and the frequencies chosen so that the transmitter intermodulation products do not degrade reception. Proper frequency management is important.

The HFICS controller output and correlator reference signals must correspondingly be filtered. The controller filters perform the same function as the transmitter filters. That is, they isolate the two transmitted frequencies. The filter in the controller reference is for phase equalization. The harmonics will also be suppressed in these filters. With such filters, the dual-channel HFICS should permit operation with surveillance receivers.

It should be noted that a single-channel HFICS can be built in much less than half the volume taken by a dual-channel HFICS. Heat dissipation will drop to 25% of the dual-channel model. The single-channel HFICS will consume one-quarter of the total RF power from the transmitters and take less than one-quarter operating power.

The current HFICS extracts a total of 400 watts from two HF transmitters. A single-channel comparable HFICS would take 100 watts. The required control power is nearly proportional to the reference RF power so that the control power decreases correspondingly in a single-channel ICS.

SECTION 6 - RECOMMENDATIONS FOR FUTURE WORK

The existing dual-channel HFICS is designed to operate with +45 dBm interference levels. It does permit reception under conditions where reception would otherwise be impossible. However, it is not optimized for operation at lower interference levels. Designing for lower interference levels permits applicable reductions in size, weight, prime power, and transmitter reference power. Significant reductions in size, weight, prime power and transmitter reference power are also possible for those cases in which a single-channel ICS is adequate.

More importantly, designing for optimum HF reception rather than for a fixed interference level will result in a marked system improvement. The general system areas under consideration are discussed in Section 5.

The HFICS should be restructured to fit one or more specific applications. This can be done without major changes in the basic system. The following data will be required for each application:

1. Transmit/receive antenna isolation over the HF band.
2. Receive antenna impedance over the receive band.
3. Minimum anticipated ambient noise over the receive band.
4. Receiver desensitization as a function of transmitter residue level at the receiver for the minimum frequency separation measured with the specific transmit signal modulation format.
5. Transmitter power, modulation format, and harmonic level.
6. Ultimate required receive sensitivity as a function of frequency.

By reducing the dual-channel HFICS to a single channel, the present volume and weight can be cut in half, the prime power requirement can be dropped from 500 to 125 watts, and the reference RF power dropped from 400 to 100 watts. The prime power and RF reference power are directly proportional to the level of the interfering signal at the receiver port. This level is, in turn, a function of space loss between the transmit and receive antennas as well as the ambient noise level at the receive antenna in an optimized system.

The addition of switched filter banks to the ICS (similar to those commonly used in modern HF receivers) will further improve performance by filtering out distortion introduced by the HFICS.

The next phase suggested is not a new HFICS but a modification of the present HFICS for one or more specific applications, followed by adequate *in situ* testing. The data obtained will permit the design of an HF interference canceller optimized for

that application. Such a canceller will perform better, occupy less volume, and take less prime and reference power than a general purpose ICS. The subassemblies used in such a canceller can be made general purpose so that spares need not present a major problem.

SECTION 7 - HIGH POWER CONTROLLERS FOR A VLF/LF ICS

In this section several different implementations are examined for VLF and LF controllers. In each case, the technique of quadrature splitting of the RF reference into two bipolar attenuators, followed by in-phase combining is preferred over phase and amplitude control. This preferred approach has the advantage of broadband control with a single controller design, and easier design of the feedback control system.

The existence of design techniques for broadband quadrature splitters and in-phase combiners in the VLF and LF ranges at the power level of interest means that the problem is reduced to one of design of the bipolar attenuator. The approaches examined for the bipolar attenuator design are discussed below; a summary of their performance characteristics is given in Table 2.

Table 2

Summary of Approaches for Implementing a Bipolar Attenuator

Approach	Max. Output Power Capability	Applicable Frequency Bands
1. Analog Multiplier	up to 50 mW	VLF and LF
2. FET Chopper	up to 10 W	VLF and LF
3. Bipolar Transistor Chopper	up to 100 W	VLF

7.1 ANALOG MULTIPLIERS

The present state of the art in analog multipliers will allow these devices to be used as bipolar attenuators for both the VLF and LF ranges. Typical devices give full power output (up to 50 milliwatts) up to 750 kHz with nonlinear distortion produces more than 55 dB down.

Low distortion is accomplished in these devices by multiplying at low levels, and then amplifying the result. This approach introduces amplifier noise at the multiplier output with typical spectral densities of 2×10^{-12} volts^2/Hz. A typical impedance level would be 2 kilohms. The noise level is thus -120 dBm/Hz or 54 dB above kTB at the output. In many cases this noise will be negligible for VLF and LF, because the received atmospheric noise is far above the thermal level. For example, at 100 kHz it is at least 75 dB above kTB, and at 10 kHz it is at least 150 dB above kTB (see Section 1.1). Data on state-of-the-art analog multipliers are given in Figure 43, which is extracted from the Analog Devices, Inc., catalog.

MULTIPLIERS/DIVIDERS (Discrete)

SPECIFICATIONS (Typical @ +25°C and ±15VDC unless otherwise specified)

	VARIABLE TRANSCONDUCTANCE TYPES			
Models[1]	**Economy 432J (432K)**	**General Purpose 426A (426K) (426L)**	**Wideband 422A (422K)**	**Accurate Wideband 429A (429B)**
Full Scale Accuracy[2]	2% (1%)	1% (1%) (0.5%)	1%	1% (0.5%)
Divides and Square Roots	YES	YES	Division requires external amp	YES
Multiplication Characteristics				
Output Function	XY/10	XY/10	XY/10	XY/10
Error, Internal Trim (±)	2% (1%) max	1% (1%) (0.5%) max	1% (1%) max	1% (0.5%) max
Error, External Trim (±)	1.0% (0.6%)	0.6% (0.6%) (0.35%)	0.7% (0.7%)	0.7% (0.3%)
Accuracy vs. Temperature (±)	0.06%/°C (0.04%/°C)	0.05%/°C (0.04%/°C max) (0.04%/°C max)	0.05%/°C (0.04%/°C max)	0.05%/°C (0.04%/°C max)
Accuracy vs. Supply (±)	0.1%/%	0.03%/%	0.05%/%	0.05%/%
Warm up Time to Specifications	1 min	1 sec	1 sec	1 sec
Output Offset (±)				
Initial	20mV (25mV max)	20mV	25mV	20mV (10mV) max
Average vs. Temperature 0 to +70°C	2mV/°C (1mV/°C)	2mV/°C (1mV/°C max) (1mV/°C max)	2mV/°C (1mV/°C max)	2mV/°C (1mV/°C max)
Average vs. Supply	10mV/%	2mV/%	1mV/%	1mV/%
Scale Factor (±)				
Initial Error	1% (0.5%)	0.5% (0.5%) (0.25%)	0.5%	0.5% (0.25%)
Nonlinearity (±)				
X Input (X = 20V p-p, Y = ±10VDC)	0.8% (0.6% max)	0.6% (0.6%) (0.25%) max	0.6% max	0.5% (0.2%) max
Y Input (Y = 20V p-p, X = ±10VDC)	0.4% (0.3% max)	0.3% (0.3%) (0.25%) max	0.3% max	0.3% (0.2%) max
Feedthrough				
X = 0, Y = 20V p-p 50Hz	80mV (50mV) p-p max	60mV (60mV) (40mV) p-p max	50mV p-p max	50mV (20mV) p-p max[3]
with external trim	30mV p-p	20mV p-p	8mV p-p	16mV (10mV) p-p
Y = 0, X = 20V p-p 50Hz	120mV (100mV) p-p max	100mV (100mV) (40mV) p-p max	100mV p-p max	100mV (30mV) p-p max
with external trim	N/A	60mV (60mV) (20mV) p-p	35mV p-p	50mV (20mV) p-p
Feedthrough vs. Temperature, each input	1mV p-p/°C	2mV p-p/°C	2mV p-p/°C	2mV p-p/°C
Bandwidth				
-3dB Small Signal	1MHz	400kHz	5MHz min	10MHz
Full Power Response	700kHz	80kHz	2MHz min	2MHz min
Slew Rate	45V/μsec	5V/μsec	120V/μsec min	120V/μsec min
Small Signal Amplitude Error (±)	1% @ 40kHz	1% at 40kHz	1% at 300kHz min	1% at 300kHz min
Small Signal Vector Error (±)	1% @ 10kHz	1% at 10kHz	1% at 50kHz min	1% at 50kHz min
Settling Time for ±10V Step	1μsec to 2%	3μsec to 1%	0.4μsec to 1%	0.5μsec to 1%
Overload Recovery	3μsec	3μsec	0.15μsec	0.15μsec
Output Noise				
5Hz to 10kHz	600μV rms	500μV rms	500μV rms	200μV rms
5Hz to 5MHz	3mV rms	2.5mV rms	2.5mV rms	1.5mV rms
Output Characteristics[4]				
Voltage at Rated Load (min)	±10V	±11V	±11V	±11V
Current (min)	±5mA	±11mA	±11mA	±11mA
Load Capacitance Limit	0.001μF	1μF	0.01μF	0.01μF
Input Resistance				
X/Y/Z Input	10MΩ/10kΩ/36kΩ	25kΩ/25kΩ/200kΩ	10kΩ/11kΩ/N/A	10kΩ/11kΩ/13kΩ
Input Bias Current				
X/Y/Z Input	2μA each	+100nA/+100nA/-50μA	+100nA each	+100nA/+100nA/±40nA
Maximum Input Voltage				
For Rated Accuracy	±10.1V	±10.5V	±10.5V	±10.5V
Safe Level	$\pm V_S$	±18V	±16V	±16V
Power Supply (V_S)				
Rated Performance	±15V	±14.7 to ±15.3V	±14.7 to ±15.3V	±14.7 to ±15.3V
Operating	±12 to ±18V	±11.5 to ±18V	±14 to ±16V	±14 to ±16V
Quiescent Current	±4.5mA	±5mA	±12mA	±12mA
Temperature Range				
Rated Performance	0 to +70°C	-25 to +85°C (0 to +70°C) (0 to +70°C)	-25°C to +85°C (0 to +70°C)	-25°C to +85°C
Operating	-25°C to +85°C	-25°C to +85°C	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Package Outline	QC-2	FA-4	F-8	FA-4
Case Dimensions	1.1" x 1.1" x 0.4"	1.5" x 1.5" x 0.6"	1.5" x 1.5" x 0.6"	1.5" x 1.5" x 0.6"
mm	(27.9 x 27.9 x 10.1)	(38.1 x 38.1 x 15.2)	(38.1 x 38.1 x 15.2)	(38.1 x 38.1 x 15.2)
Prices (1-9)	$30 ($46.50)	$47.50 ($62) ($68)	$120 ($142)	$109 ($139)
(10-24)	$28 ($44.50)	$45.00 ($60) ($65)	$114 ($131)	$104 ($129)

NOTES:

[1] Parentheses indicate specification for the high performance (K or L version) model of each multiplier when it differs from the J or A version. For example, order model 427J for 0.25% accuracy, model 427K for 0.2% accuracy.

[2] All accuracy and error specifications, when expressed as percentages, refer to % of full scale (10V).

[3] Model 424 available for $22 additional on printed circuit board with preadjusted trim pots. Card socket supplied. Order model 425J or 425K.

FIGURE 43

ANALOG MULTIPLIER DATA, FROM ANALOG DEVICES, INC.

7.2 CHOPPED BIPOLAR ATTENUATOR

In general, the nonlinear distortion and power handling problems of a solid state device are worse when the device is operated in its linear region, compared to switched operation. In order to overcome these problems, switched operation is examined here to be used in a bipolar attenuator based on biphase ($\pm$) variable duty cycle chopping to control both polarity and attenuation.

Figure 44 shows the chopped bipolar attenuator. The RF signal is multiplied by a rectangular signal ($\pm$1). The duty cycle controls the polarity and amplitude of the RF component in the product. The attenuated RF component is isolated by the lowpass filter (LPF).

Figure 45 shows the resulting waveforms. (1) is the RF signal before chopping. (2.1) is a chopping signal at a frequency above twice the RF, with the (+1) duty cycle set much above 50% for a large in-phase component. (2.2) is the chopped signal and (2.3) is the output with all frequency components above the RF filtered out.

Similarly, the (3) set of waveforms shows that with $\pm$1 symmetrical chopping at 50% duty cycle, the filtered output is zero (maximum attenuation). The (4) set of waveforms shows the 180° phase shift (waveform inversion) resulting from altering the chopping signal duty cycle so that it is predominantly negative (+1 less than 50% duty cycle).

A spectral illustration of the variable duty cycle chopper technique is illustrated in Figure 46. Since the output of the chopper is the product of the RF reference and chopper waveforms, the spectrum of the chopper output is the convolution of the Fourier transforms of the reference and chopper waveforms. The transform of the chopper waveform has spectral lines at the chop frequency f_c; has a (sin f)/f envelope whose first zero crossing varies from f_c to infinity depending upon the duty cycle; and has a DC component A_0 that varies from -1 to +1 as the +1 duty cycle varies from 0 to 100%. The chopper is really a balanced mixer in which the balance to the RF input is varied by the duty cycle of the chopping input.

The desired output component is at f_0. Its amplitude is seen to be proportional to A_0. A_0 is directly proportional to the chopping duty cycle; it is zero when the duty cycle is 50%.

The implementation of the bipolar attenuator in this controller would consist of a transformer with a center-tapped secondary and a single-pole double-throw switch (Figure 47). Lowpass filtering then provides the desired output.

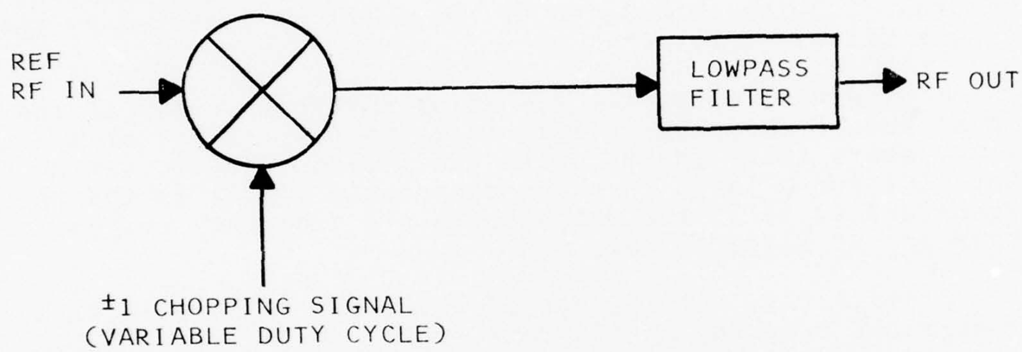


FIGURE 44

FUNCTIONAL DESCRIPTION OF CHOPPED
BIPOLAR ATTENUATOR

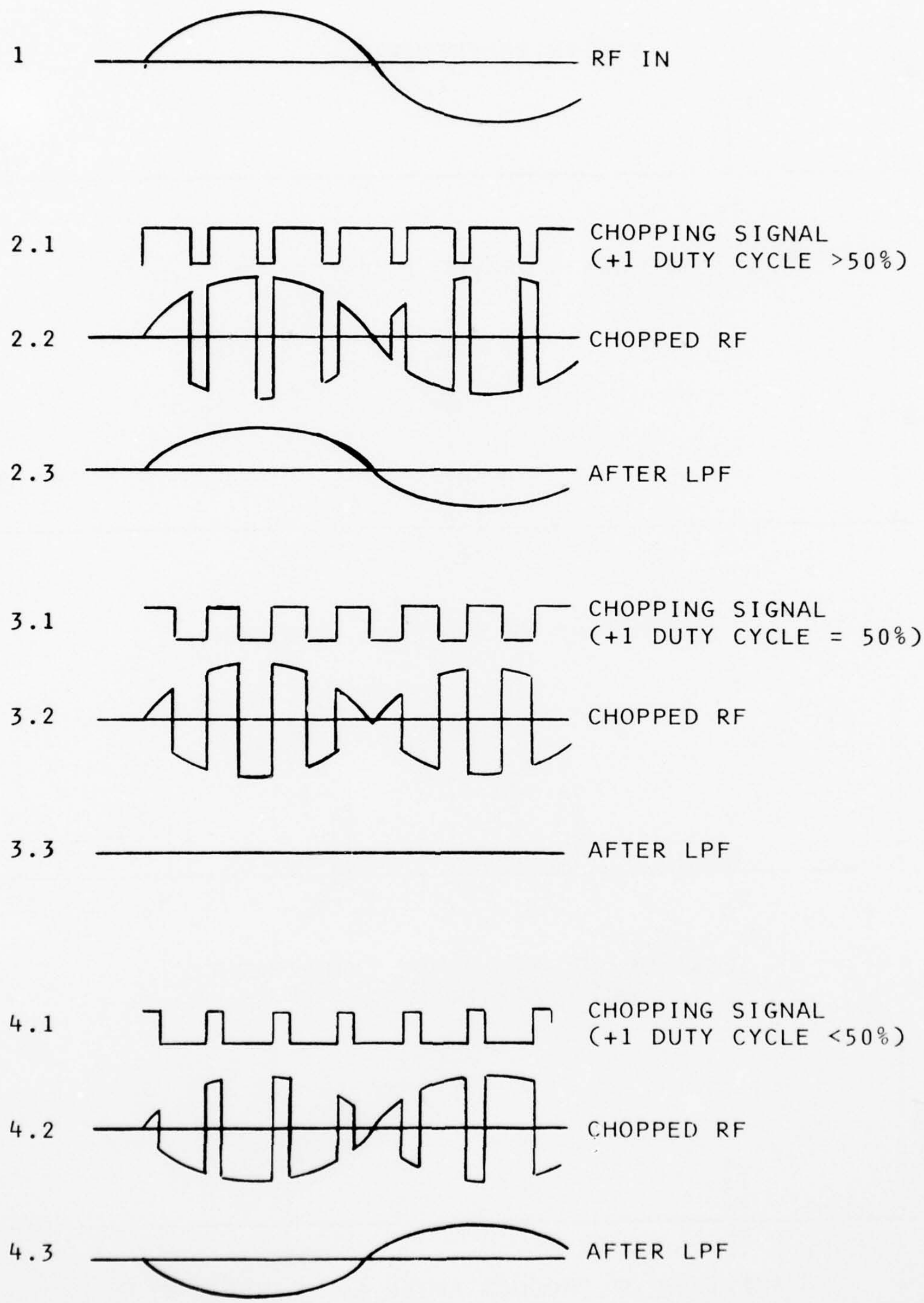


FIGURE 45

CHOPPED BIPOLAR ATTENUATOR WAVEFORMS

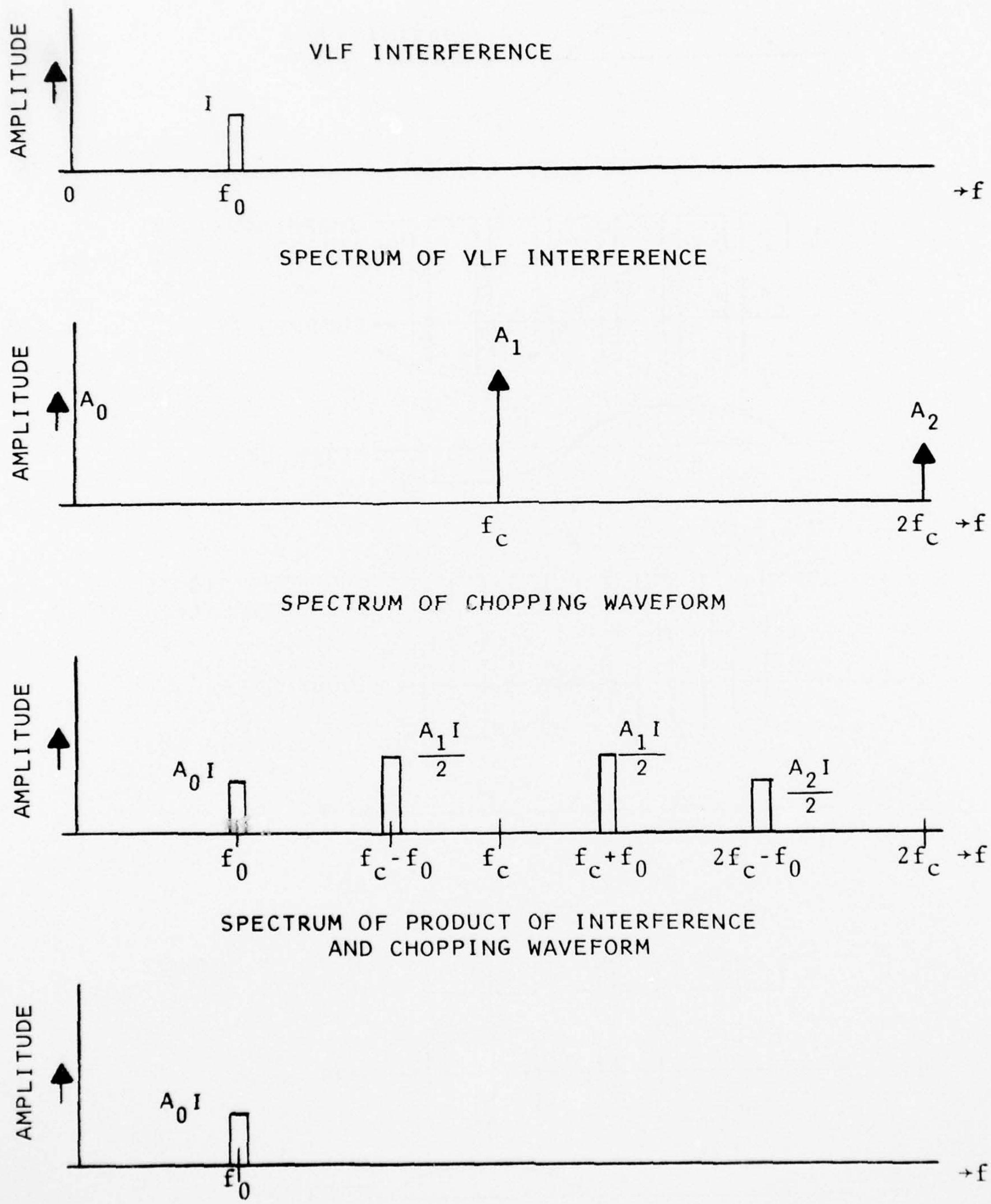


FIGURE 46
SPECTRAL ILLUSTRATION OF VARIABLE DUTY CYCLE CHOPPER BIPOLAR ATTENUATOR

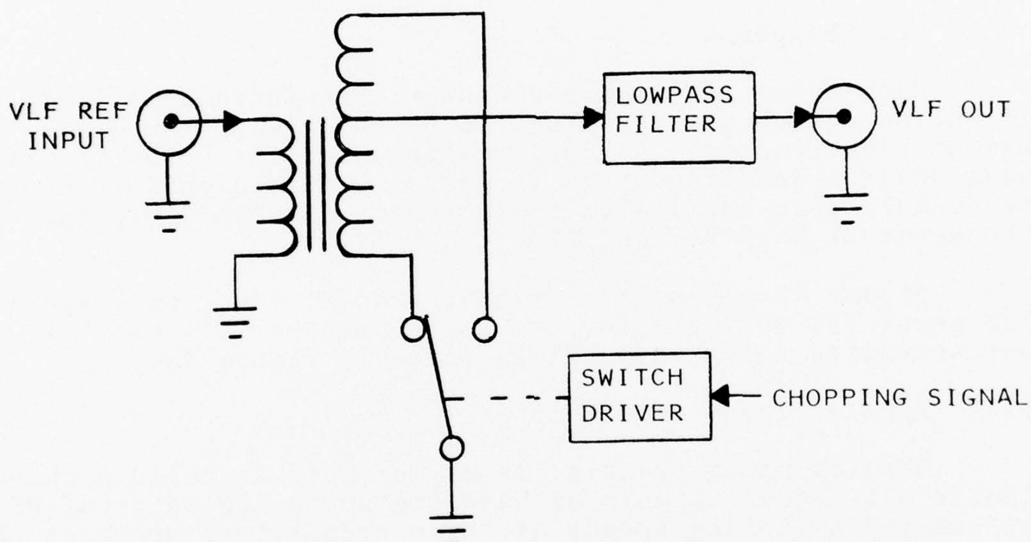


FIGURE 47
CHOPPER BIPOLAR ATTENUATOR BLOCK DIAGRAM

The polarity of the output depends on the switch position. It is in-phase with the primary when the switch is thrown to the left (as shown) and 180° out-of-phase when the switch is thrown to the right.

The single-pole double-throw switch is the critical control element. While the basic elements, in the form of high-speed, high-power switching transistors are well developed, their combination into a low distortion, bipolar SPDT switch will take some design effort. However, operating the transistors in either the saturated or cut-off states instead of allowing them to operate in the linear region provides lower distortion and reduces the prime power required.

7.2.1 FET Chopper

High-power FET's have recently been introduced [3,4] which will allow a high-speed chopper to be built with low drive-current requirements. A bipolar attenuator can be built with these devices handling up to 10 watts. Their high switching speeds make them applicable to implement a chopped bipolar attenuator at both VLF and LF.

Figure 48 gives data from Siliconix, Inc., on a typical high power FET suitable for use in the chopper circuit. A circuit schematic using this FET is given in Figure 49.

7.2.2 Bipolar Transistor Chopper

Bipolar power transistors may be used to build a chopped bipolar attenuator capable of handling up to 100 watts of RF. The limited switching speeds of these transistors prevents their use in chopped bipolar attenuators at frequencies above VLF.

State-of-the-art switching transistors are typified by the General Semiconductor Industries, Inc., data given in Figure 50. A circuit schematic using such switching transistors is given in Figure 51.

[3] L. Schaeffer, "Use FETs to Switch High Currents," *Electronic Design 9*, 26 April 1976, p. 66.

[4] M. Vander Kooi, L. Ragle, "MOS Moves into Higher Power Applications," *Electronics*, 24 June 1976, p. 98.

VMP 4
MOSPOWER™ FET

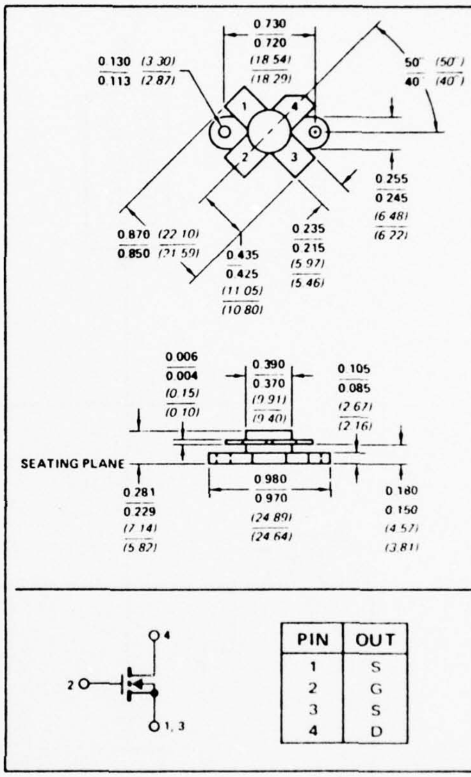
FIGURE 48

N-CHANNEL ENHANCEMENT-MODE VHF POWER MOSFET

Preliminary Data July 1976

Especially suited for medium-power VHF amplifiers operating in class B, C or D service. Also in high dynamic range, small signal VHF amplifiers.

- No Thermal Runaway
- No Secondary Breakdown
- Withstands Any VSWR
- High Gain 10 dB Min @ 200 MHz
- No Minority Carrier Storage
- Low Small-Signal Noise Figure
- High Two-Tone Intermodulation Intercept Point



PIN	OUT
1	S
2	G
3	S
4	D

ABSOLUTE MAXIMUM RATINGS

Drain-Source Breakdown Voltage BV_{DSX} . . . . . 60 V
Source-Gate Breakdown Voltage BV_{SGX} . . . . . 20 V
Drain ON Current $I_{D(on)}$ . . . . 1.6 A
Total Device Dissipation @ $T_C = 25°C$ . . . . . . 35 W
Power Derating . . . . 280 mW/°C
Storage Temperature Range . . . . −55 to +150°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristics		Min	Typ	Max	Unit	Test Conditions
1	BV_{DS}	Drain-Source Breakdown	36			V	$V_{GS} = 0$; $I_D = 100\ \mu A$
2	BV_{GSO}	Gate-Source Breakdown	20				$V_{DS} = 0$; $I_G = 10\ \mu A$
3	$I_{D(on)}$	Drain ON Current			1.6	A	$V_{DS} = 24$ V; $V_{GS} = 5$
4	C_{os}	Output Capacity			35	pF	$V_{DS} = 24$ V; $V_{GS} = 0$
5	G_{ps}	Common-Source Power Gain	10			dB	$V_{DS} = 36$ V; $I_D = 0.8$ A; f = 200 MHz
6	NF	Small-Signal Spot Noise Figure		2.5			$V_{DS} = 24$ V, $I_D = 0.4$ A; f = 150 MHz

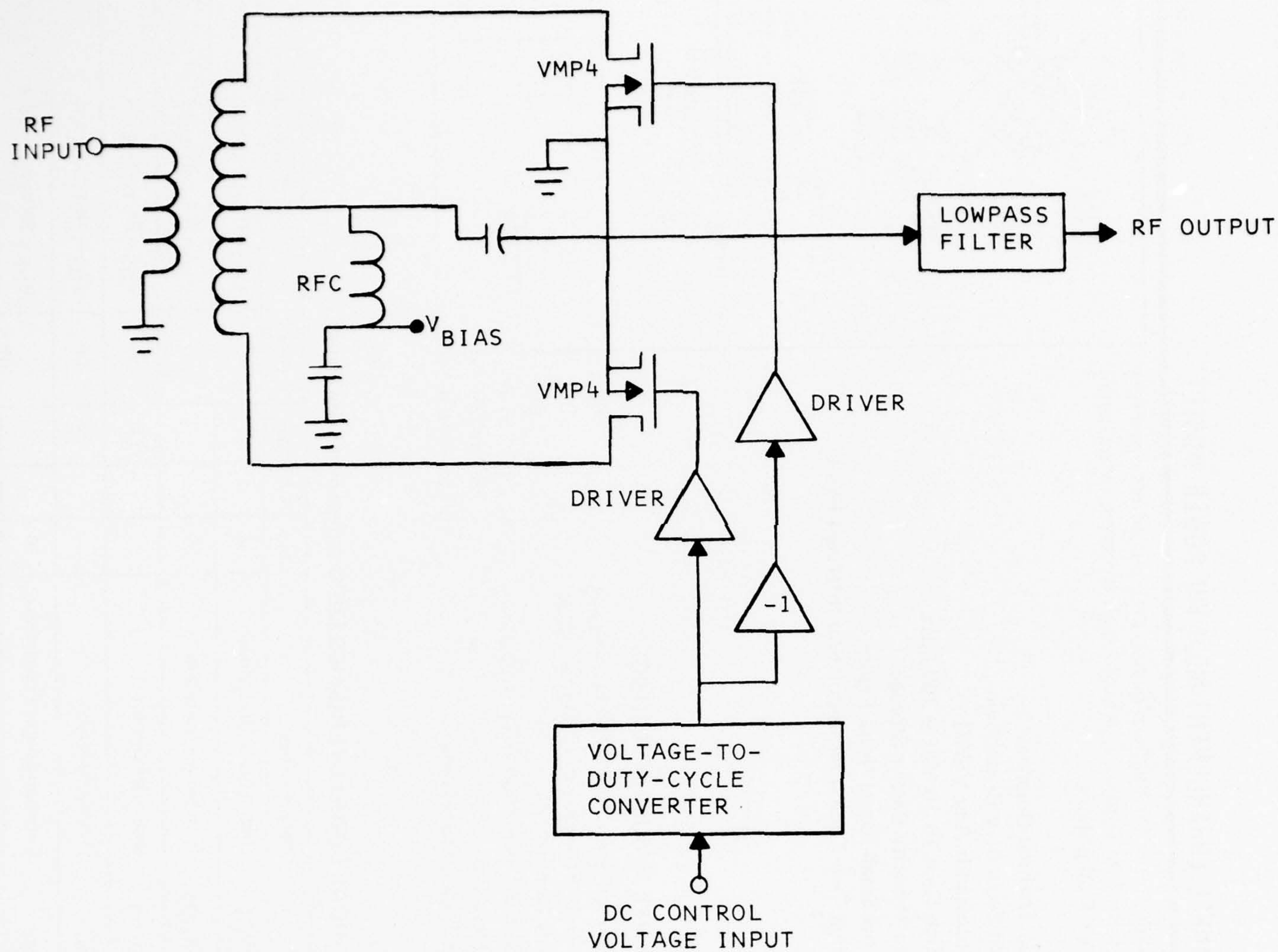


FIGURE 49

FET CHOPPER BIPOLAR ATTENUATOR

PRELIMINARY

GENERAL SEMICONDUCTOR INDUSTRIES, INC..

FIGURE 50

XGSR10025
XGSR10030
XGSR10035

NPN DIFFUSED SILICON C2R™ FAST SWITCHING POWER TRANSISTOR

ABSOLUTE MAXIMUM RATINGS	XGSR10025	XGSR10030	XGSR10035	UNITS
COLLECTOR-BASE VOLTAGE	300	350	400	VOLTS
COLLECTOR-EMITTER VOLTAGE	250	300	350	VOLTS
EMITTER-BASE VOLTAGE	7.0	7.0	7.0	VOLTS
COLLECTOR CURRENT-CONT	10	10	10	AMPS
COLLECTOR CURRENT-PEAK	20	20	20	AMPS
BASE CURRENT-CONT.	5.0	5.0	5.0	AMPS
TOTAL POWER DISSIPATION @100°C Case	100	100	100	WATTS
θ j-c	0.75	0.75	0.75	°C/W
JUNCTION TEMPERATURE		-65 to +175		°C
STORAGE TEMPERATURE		-65 to +200		°C

ELECTRICAL CHARACTERISTICS @ +25°C AMBIENT UNLESS OTHERWISE NOTED

	XGSR10025		XGSR10030		XGSR10035			
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
BV_{CBO}	300		350		400		VOLTS	I_C = 10mA
BV_{CEO}	250		300		350		VOLTS	I_C=50mA
BV_{EBO}	7.0		7.0		7.0		VOLTS	I_E = 1.0mA
BV_{CEX}	300		350		400		VOLTS	I_C = 50mA, V_{BE} = −1.5V (Fig. 4)
BV_{CER}	275		325		375		VOLTS	I_C = 50mA, R = 100Ω (Fig. 4)
I_{CBO}		500		500		500	µA	V_{CB} = 80% V_{CB} Rated
I_{EBO}		100		100		100	µA	V_{EB} = 5.0V
I_{CEO}		1.0		1.0		1.0	mA	V_{CE} = 80% V_{CE} Rated
h_{FE} *	20		15		10			V_{CE} = 5.0V, I_C = 10A
h_{FE} TYP *	25		20		15			V_{CE} = 5.0V, I_C = 10A
$V_{CE\,(sat)}$ *		0.8		0.8		0.8	VOLTS	I_C = 10A, I_B = 2.0A
$V_{BE\,(sat)}$ *		1.3		1.3		1.3	VOLTS	I_C = 10A, I_B = 2.0A
$\|h_{fe}\|$	2.5		2.5		2.5			V_{CE} = 10V, I_C = 1.0A, f = 10 MHz
C_{obo}		350		350		350	pF	V_{CB} = 10V, f = 1MHz
t_{on}		0.2		0.2		0.2	µs	V_{CC} = 100V, I_C = 10A, I_{B_1} = 1.0A, I_{B_2} = 1.0A — REFER TO FIGURE 3
t_s		1.5		1.5		1.5	µs	
t_f		0.5		0.5		0.5	µs	
TYPICAL STORAGE TIME					400		ns	I_C = 10A, I_{B_1} = I_{B_2} = 1.0A

*Pulse measurement conditions: Length = 300 µs, Duty cycle ≤ 2%, using separate current carrying and voltage sensing leads

TO-3 PACKAGE

GENERAL SEMICONDUCTOR INDUSTRIES, INC. 2001 West Tenth Place, Tempe, Arizona 85281 • 602 968 3101 • TWX910 950 1942
Mailing Address P.O. Box 3078

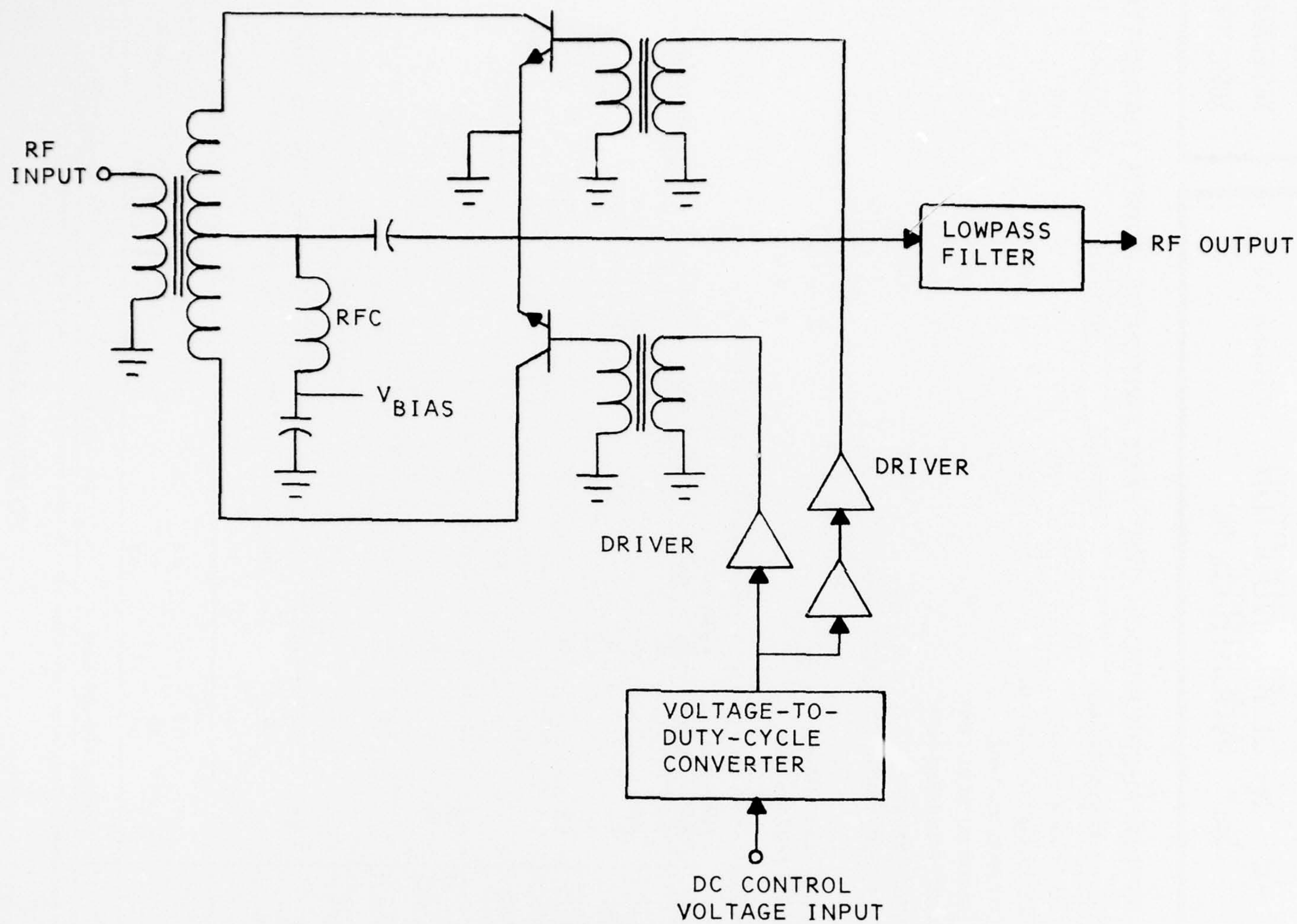


FIGURE 51

TRANSISTOR CHOPPER BIPOLAR ATTENUATOR